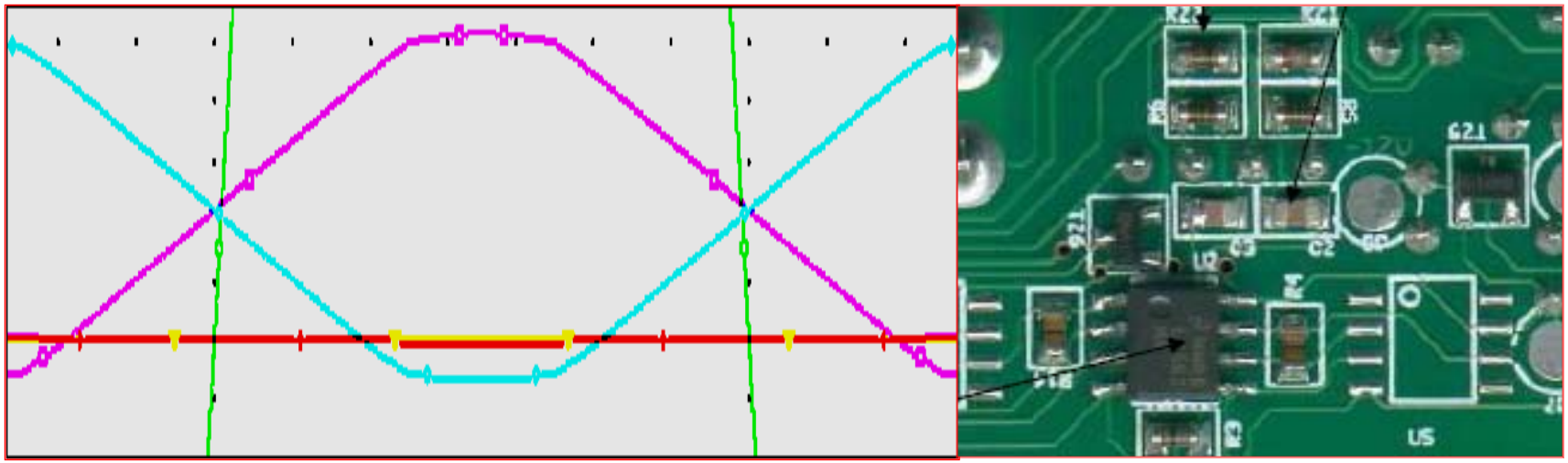
VISOKA ŠKOLA ELEKTROTEHNIKE I RAČUNARSTVA STRUKOVNIH STUDIJA-VIŠER, BEOGRAD

STUDIJSKI PROGRAM: NOVE ENERGETSKE TEHNOLOGIJE

SPECIJALISTIČKE STUDIJE

PREDMET: UPRAVLJANJE ELEKTROENERGETSKIM PRETVARAČIMA

OSNOVNA KONTROLNA ELEKTRONSKA KOLA



Predmetni profesor: Dr Željko Desptović, dipl.el.inž

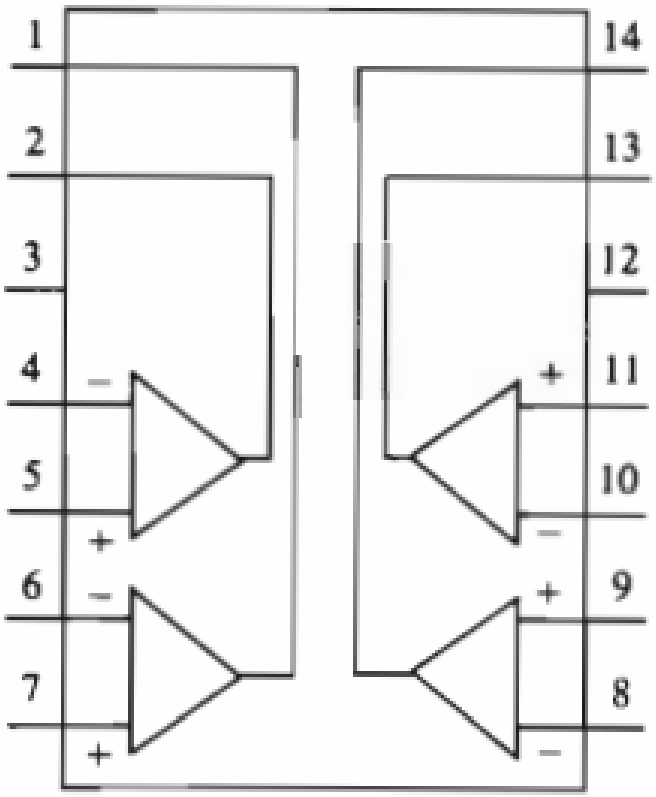
UVOD

Biće date osnovne predstave o radu osnovnih elektronskih sklopova koji se najčešće koriste u upravljačkim kolima elektroenergetskih pretvarača:

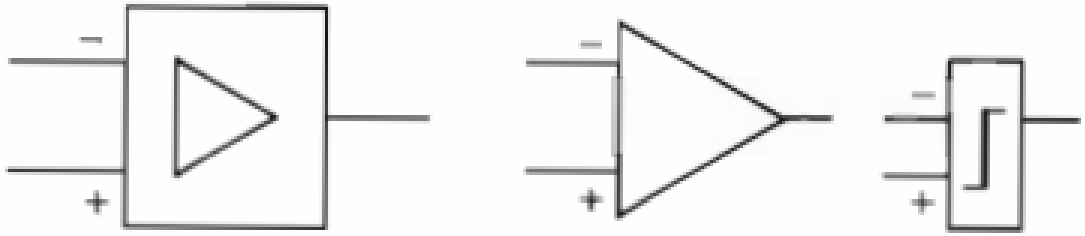
1. Komparatori
2. Bistabilna kola
3. Pojačavači (invertujući i neinvertujući)
4. Generatori naponske rampe, PI regulatori
5. CMOS invertori
6. Šmit trigeri
7. Flip-flopovi
8. Monostabilna i bistabilna kola
10. Analogniprekidači
11. Analogni množači

KOMPARATORI

LM139/239/339

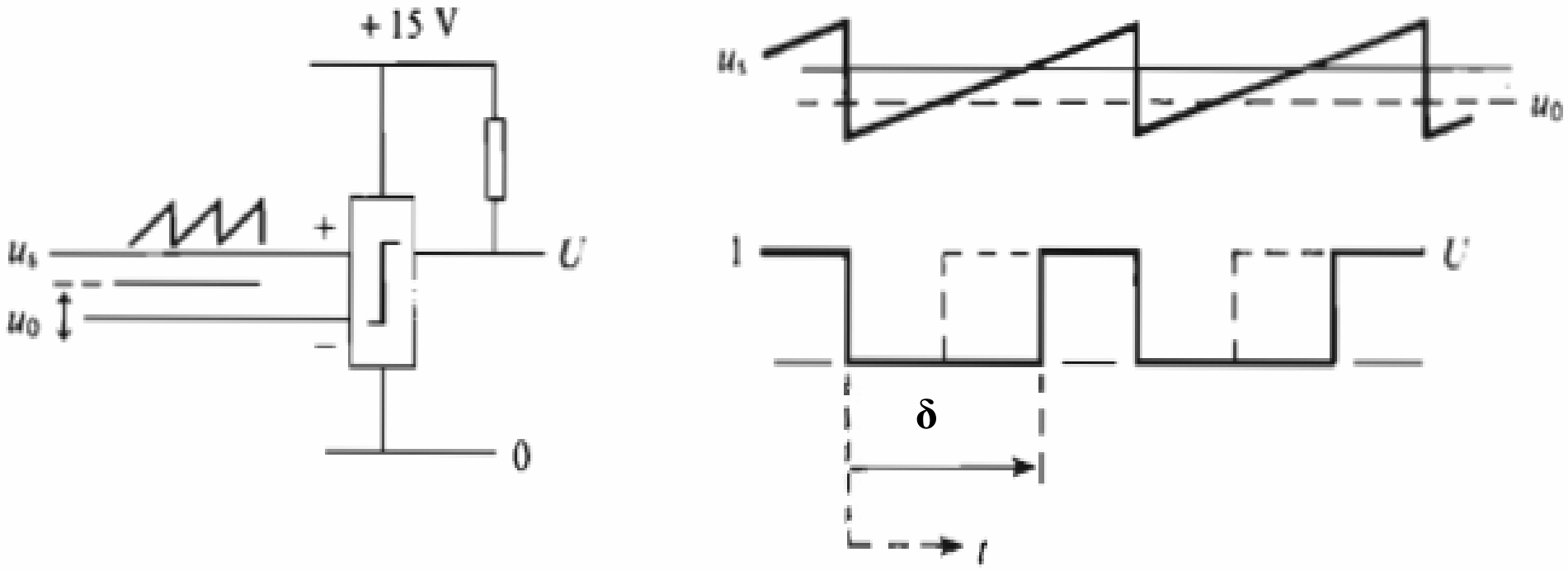


PIN out



simboli

PWM (Pulse Width Modulator) sa komparatorom

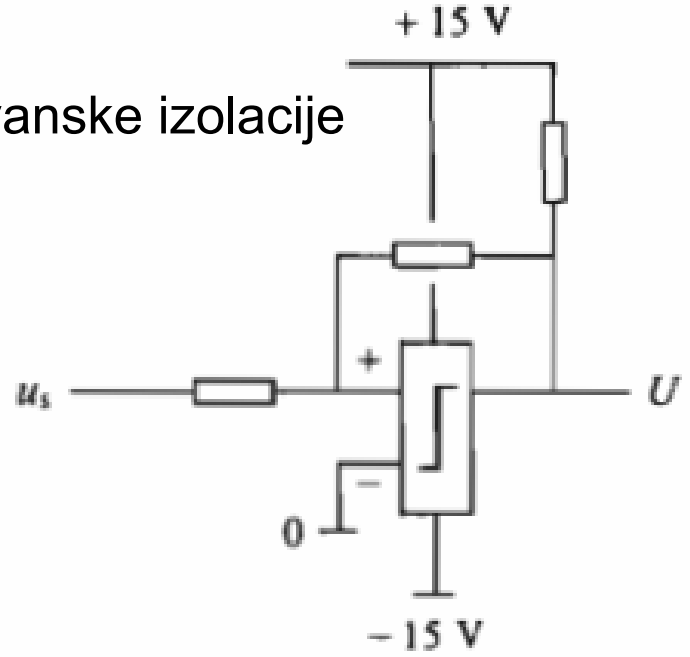


Širinsko impulsni modulator: Promenom jednosmernog nivoa u_o dobija se promena koeficienta radnog režima (duty-cycle) δ

ZCD (Zero Crosing Detector)/ Detektori prolaska napona kroz nultu vrednost

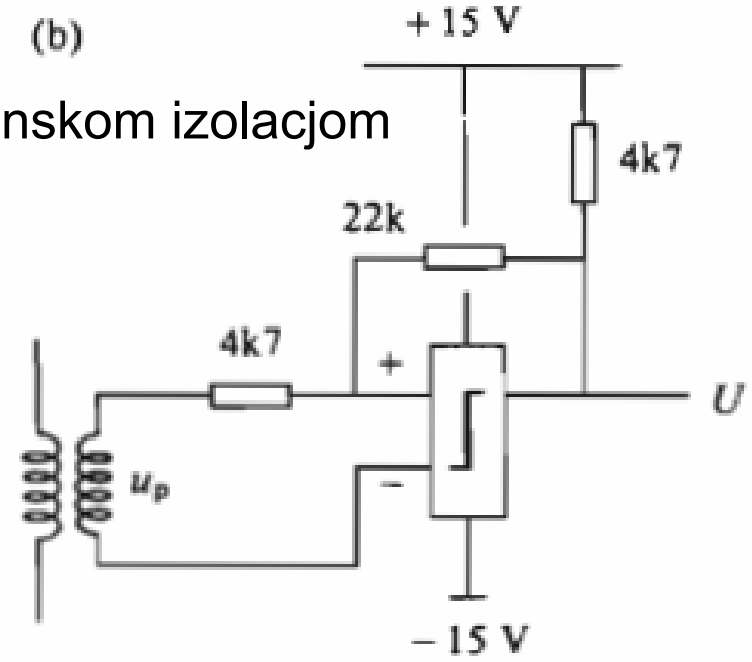
(a)

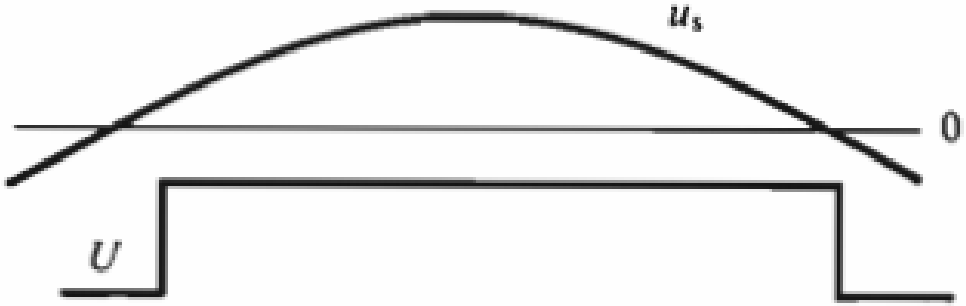
Bez galvanske izolacije

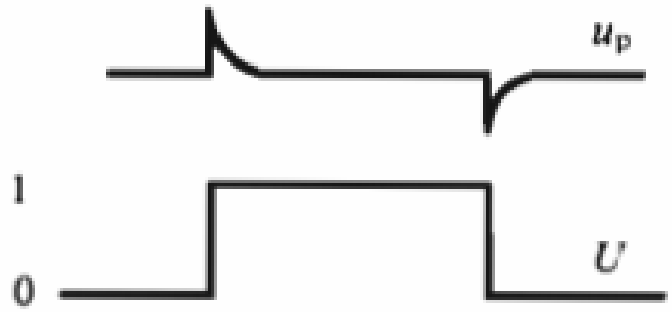


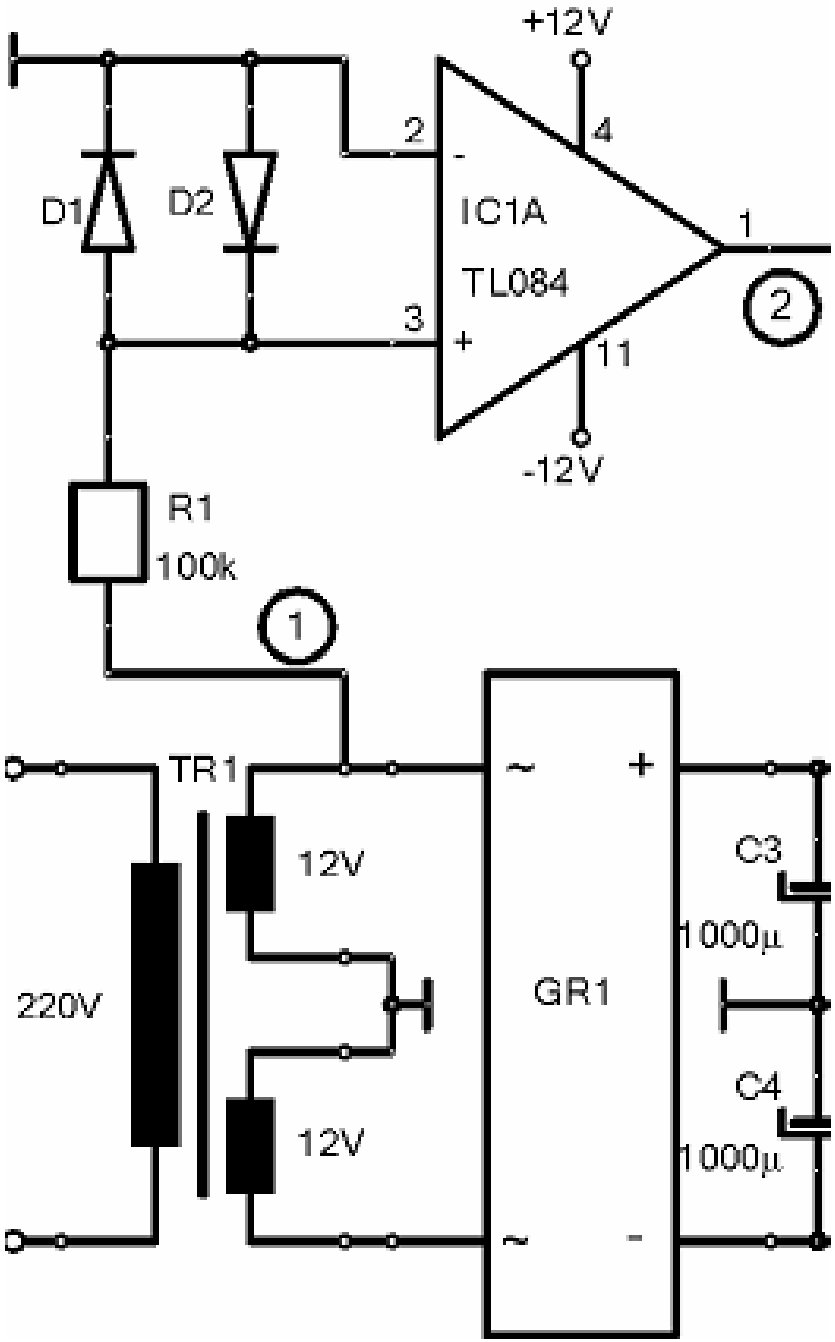
(b)

Sa galvanskom izolacjom

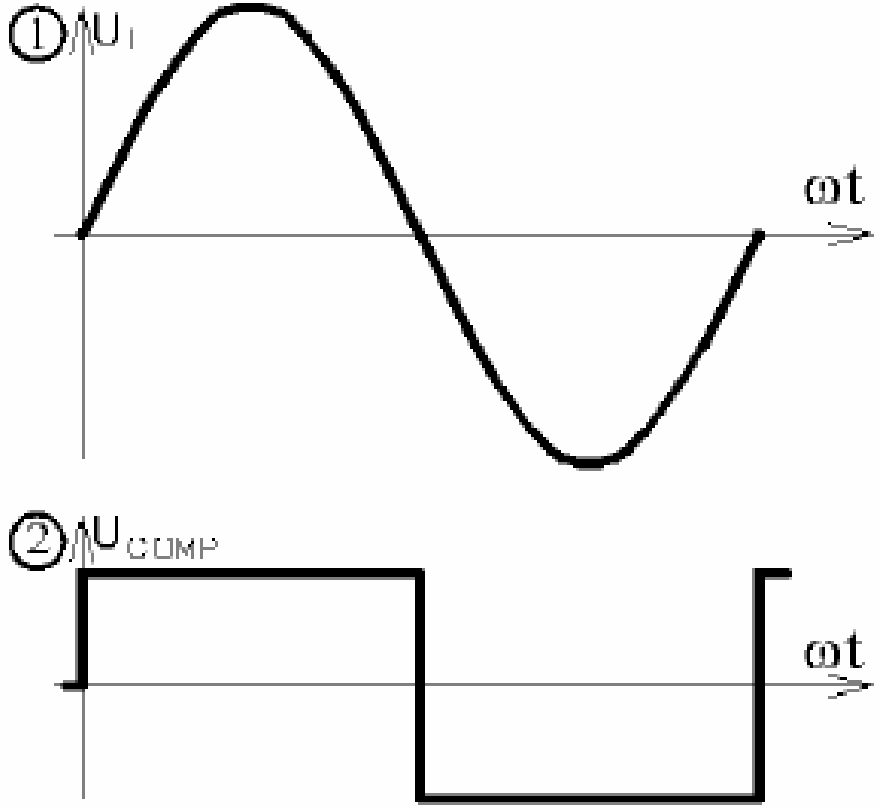






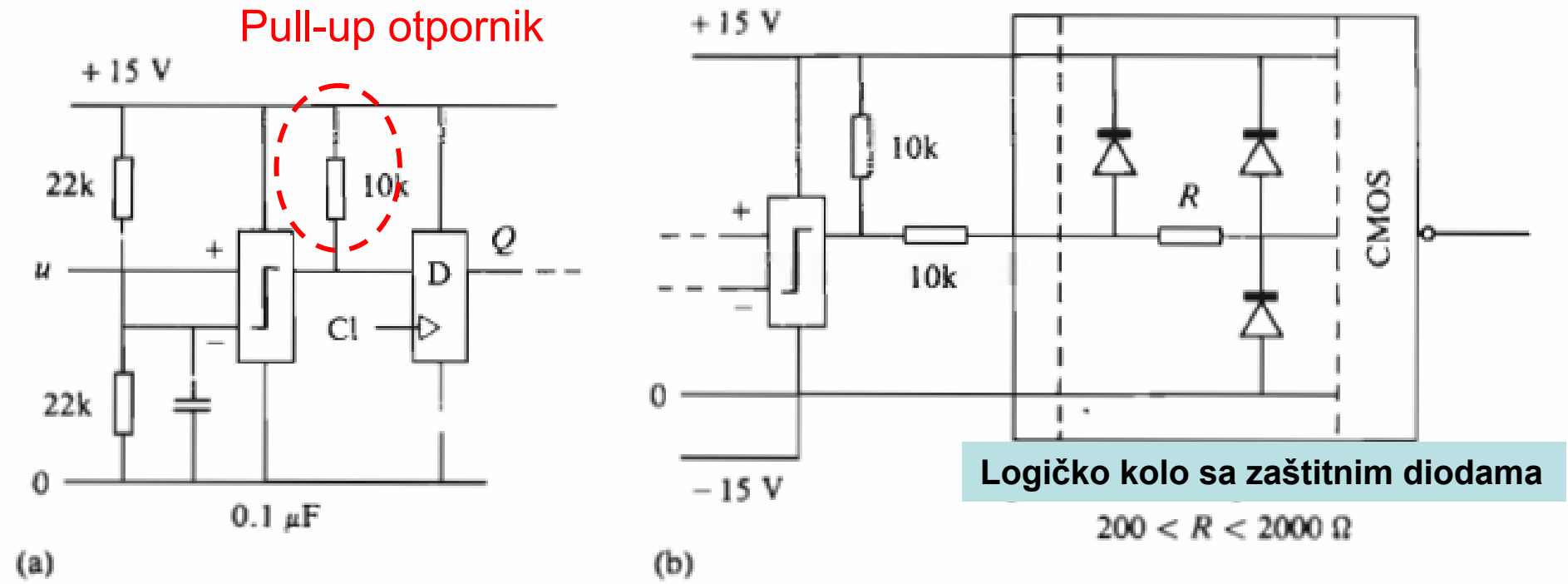


TIPIČMA PRIMENA:
SINHRONIZACIJA SA MREŽOM



Izobličenja koja unosi punjenje kondenzatora C3 i C4, ne unose smetnje jer se punjenje ostvaruje u vršnim vrednostima napona sekundara TR1

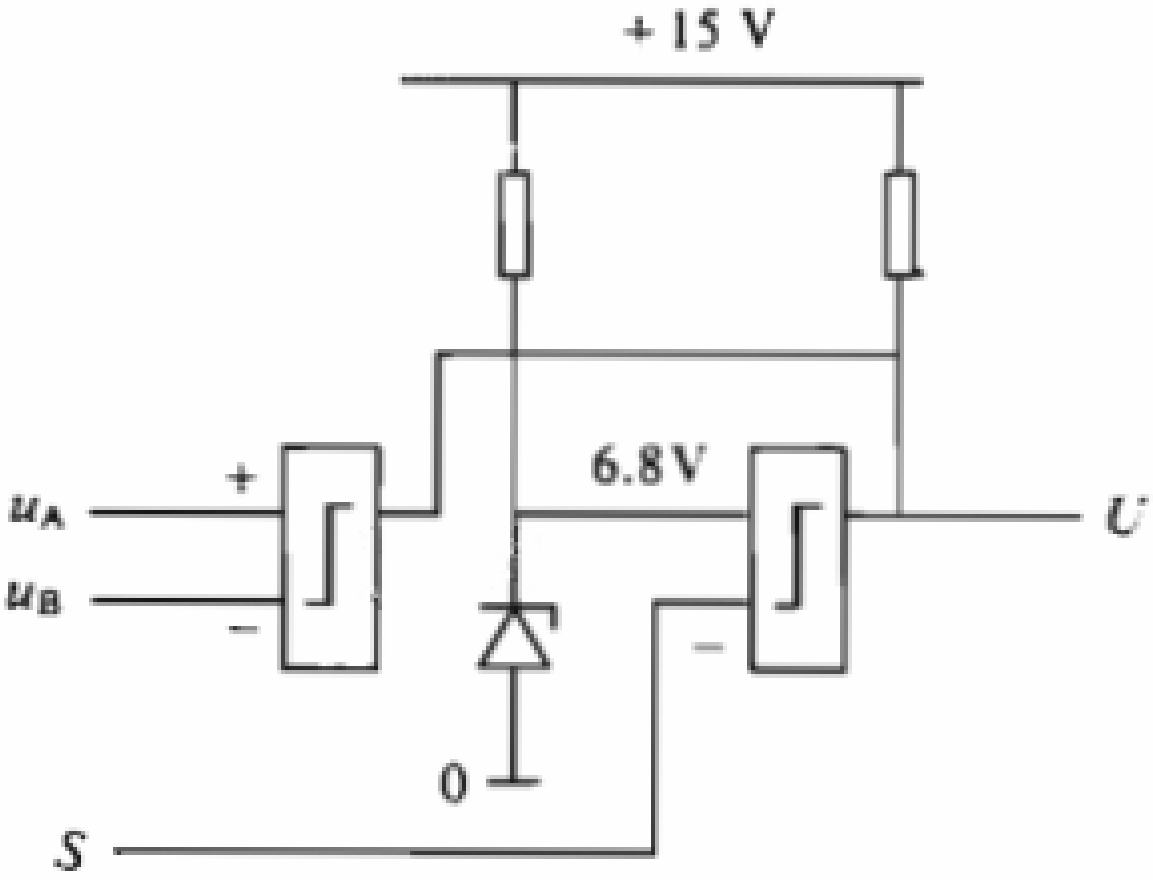
POVEZIVANJE KOMPARATORA I LOGIČKIH KOLA



Povezivanje sa TTL

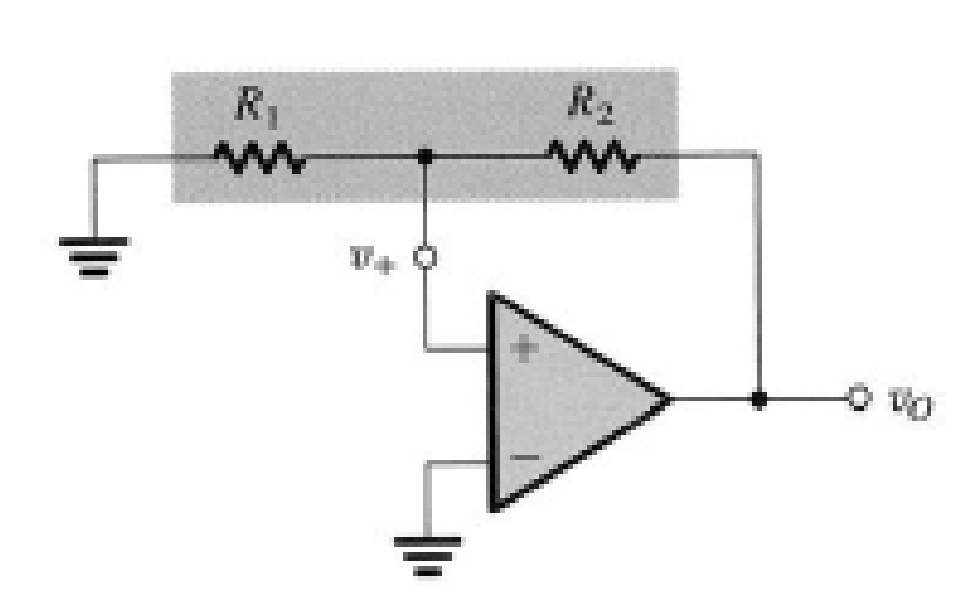
Povezivanje sa CMOS

TIPIČNA PRIMENA DVA KOMPARATORA



U=1 ako je S=0 i ua > ub

BISTABILNO KOLO



Stabilna stanja:

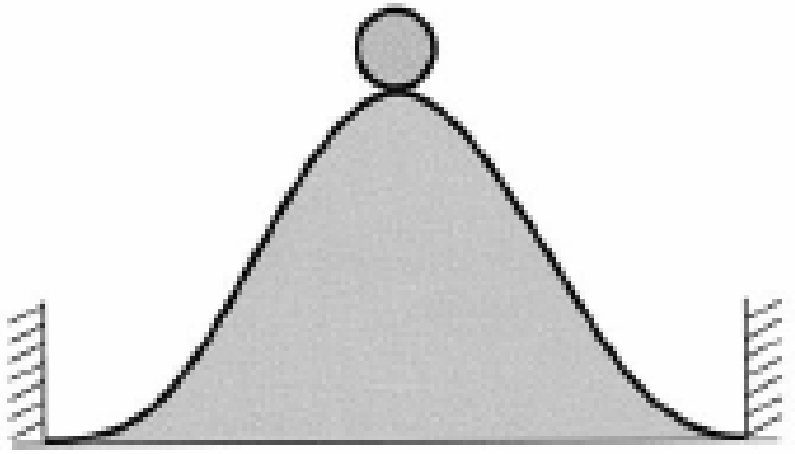
$$v_O = L_+$$

$$v_+ = L_+ R_1/(R_1+R_2)$$

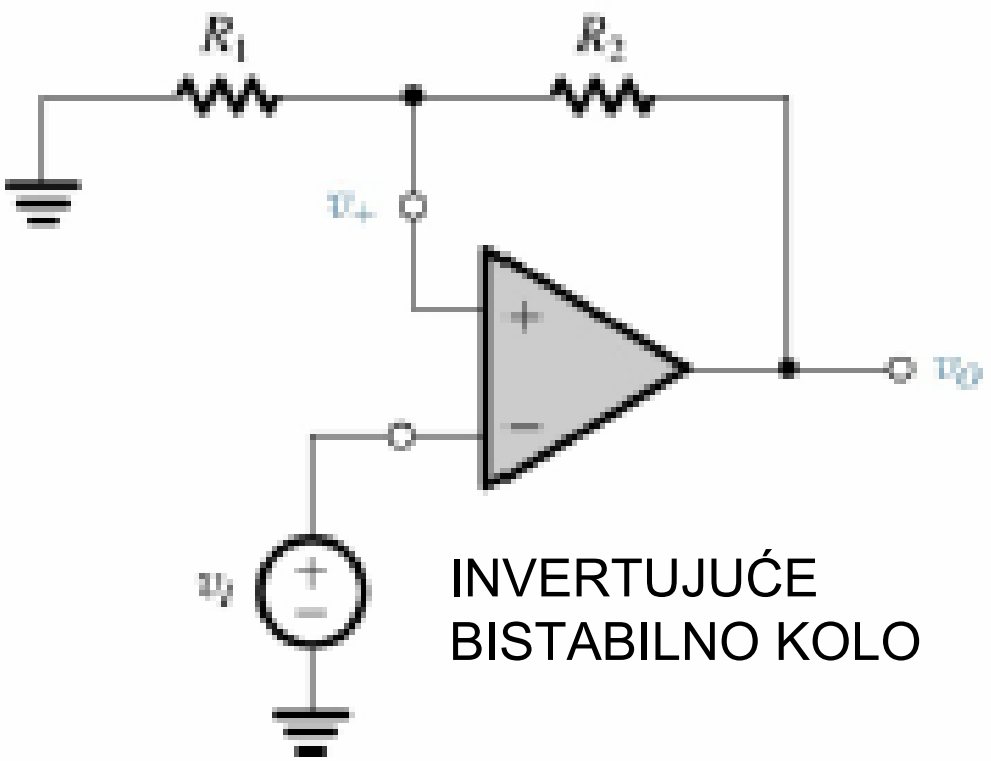
$$v_O = L_-$$

$$v_+ = L_- R_1/(R_1+R_2)$$

Mehanička analogija



PRENOSNA KARAKTERISTIKA BISTABILNOG KOLA

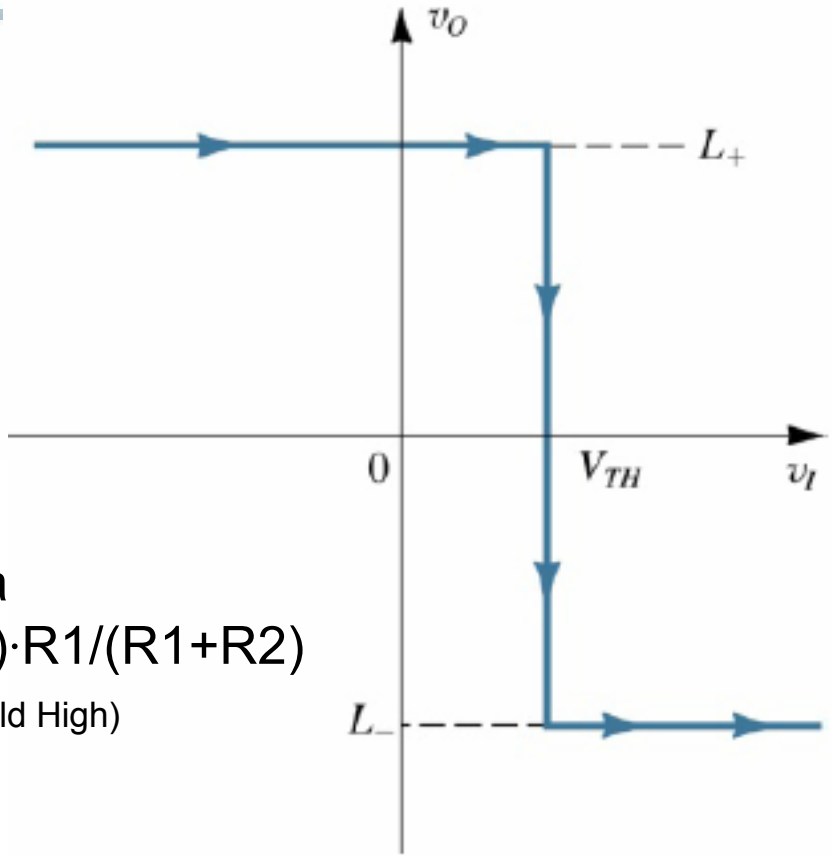


INVERTUJUĆE
BISTABILNO KOLO

Početno stanje:

$$v_O = L_+$$

$$v_+ = L_+ R_1/(R_1+R_2)$$

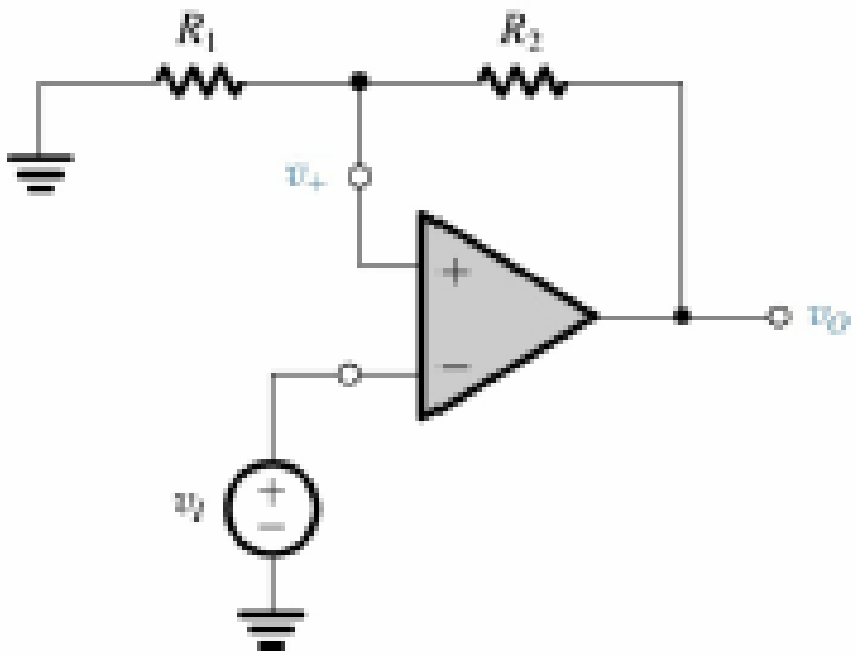


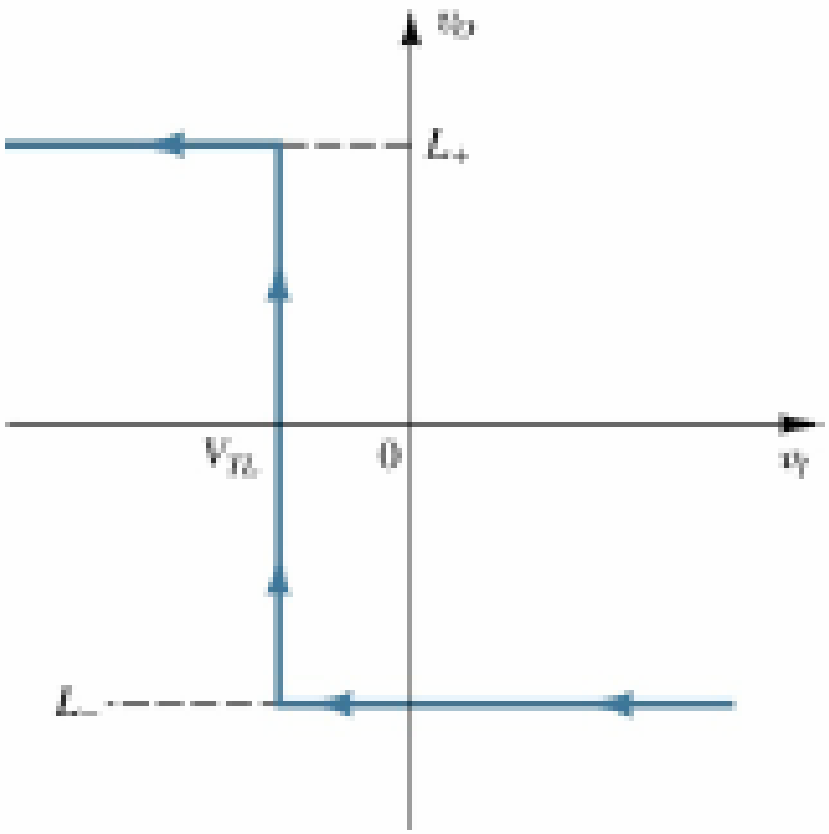
Izlazni napon menja stanje sa L+ na L- kada
ulazni napon postanje veći od vrednosti (L+)·R1/(R1+R2)
Ova rednost se zove gornji prag ili V_{TH} (Thresold High)

Početno stanje:

$$v_O = L_-$$

$$v_+ = L_- R_1/(R_1+R_2)$$



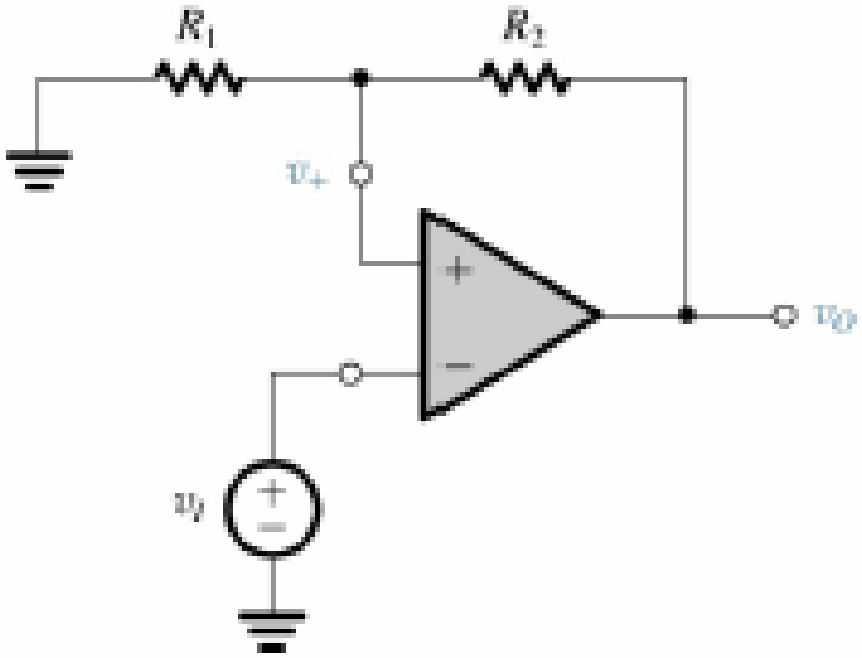


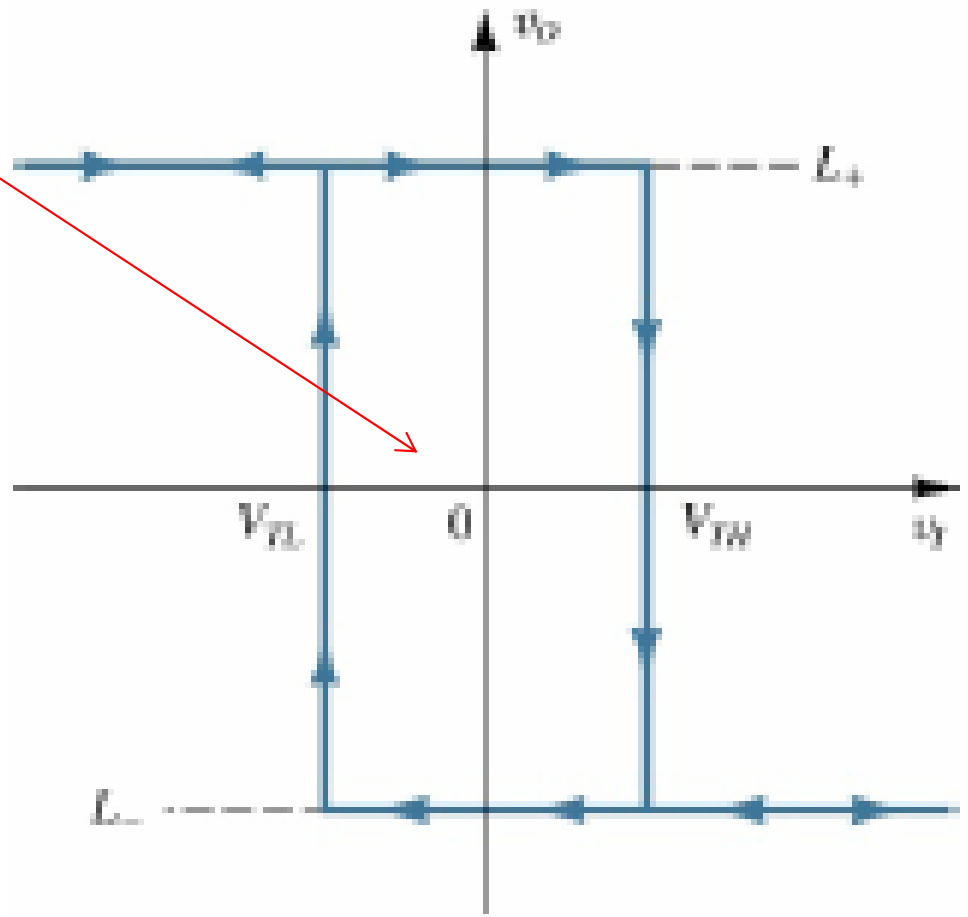
Izlazni napon menja stanje sa L- na L+kada ulazni napon postanje manji od vrednosti (L-)·R1/(R1+R2).
Ova rednost se zove donji prag ili V_{TL} (Thresold Low)

KOLO DAKLE IMA HISTEREZIS

ČIJA JE ŠIRINA:

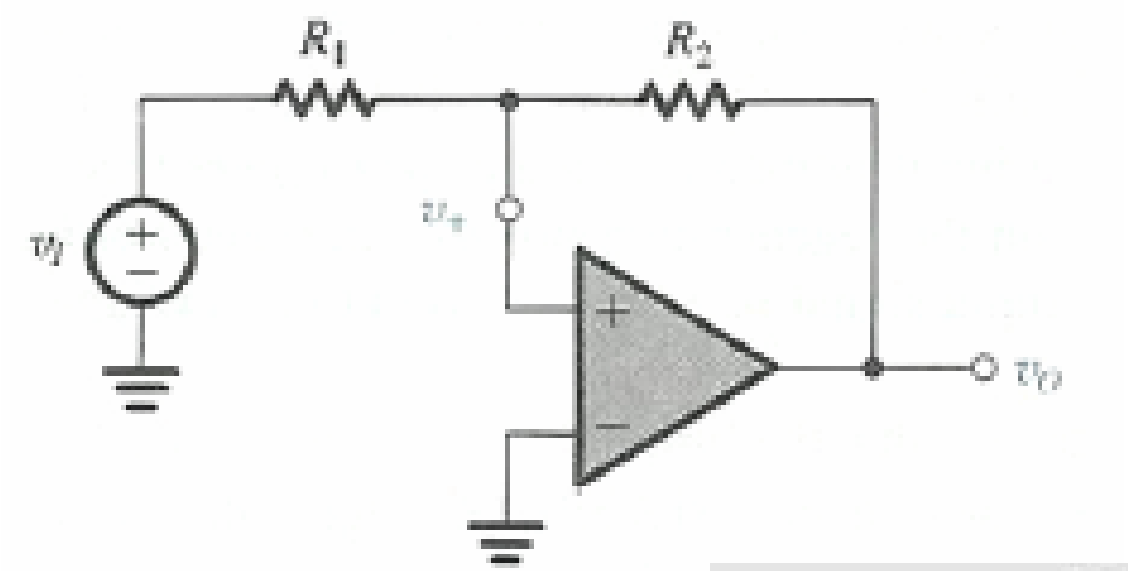
$$(V_{TH} - V_{TL})$$



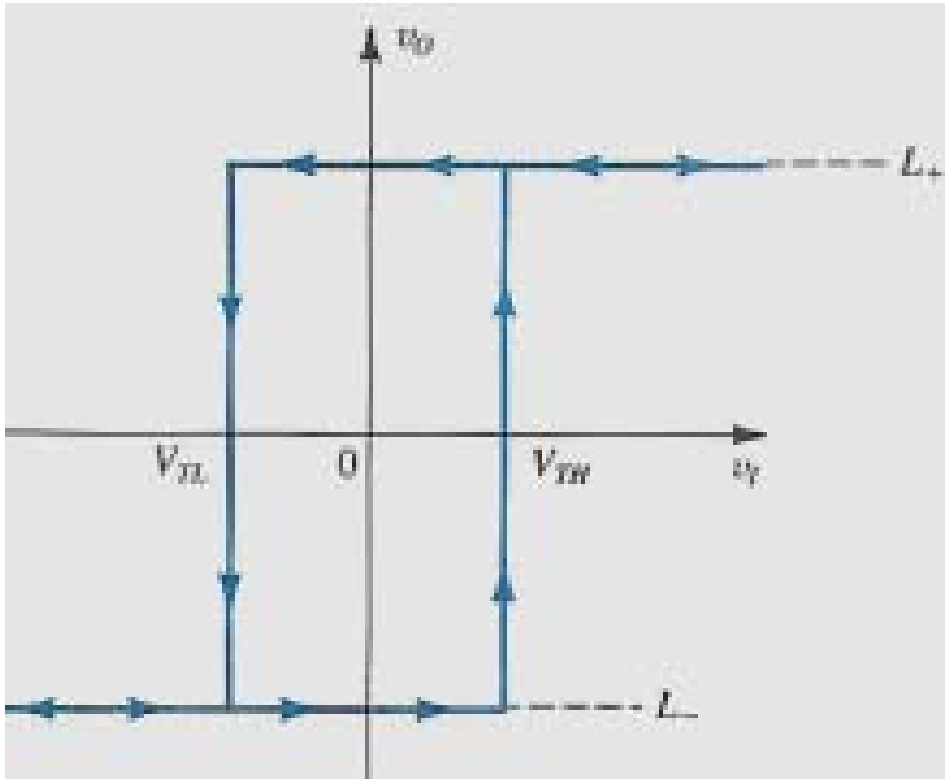


PRENOSNA KARAKTERISTIKA INVERTUJUĆEG BISTABILNOG KOLA

NEINVERTUJUĆE BISTABILNO KOLO

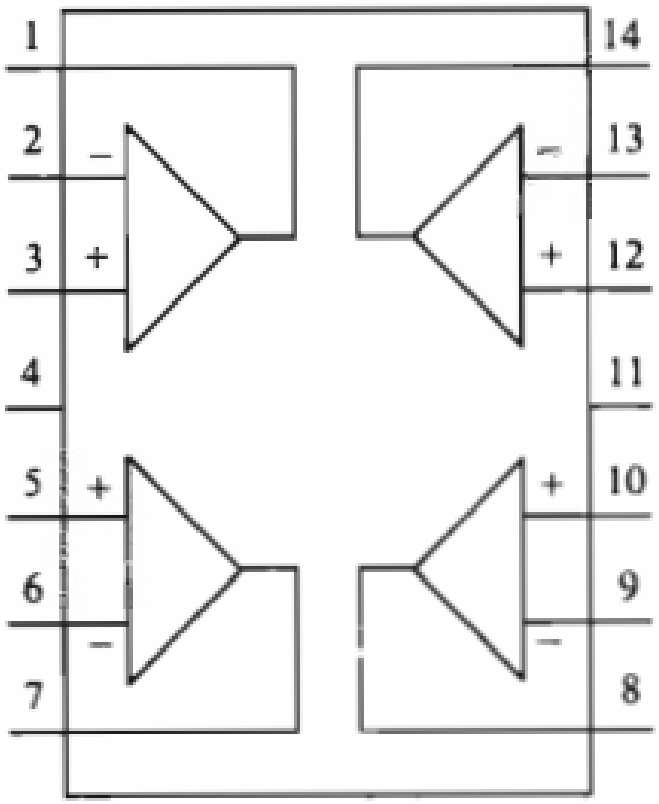


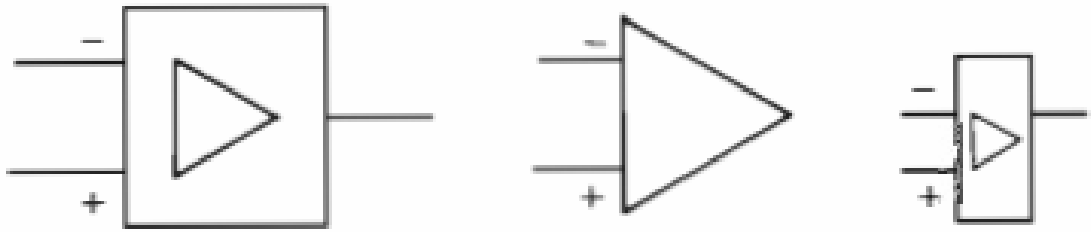
PRENOSNA FUNKCIJA



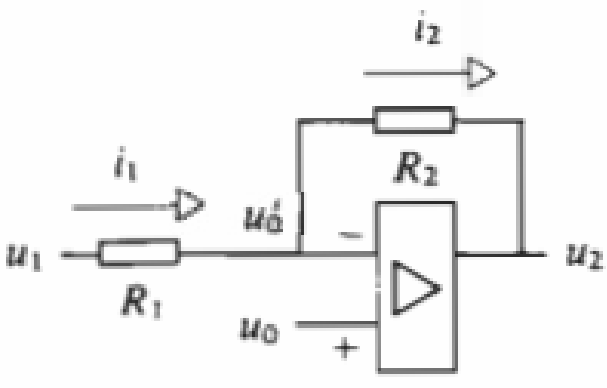
OPERACIONI POJAČAVAČ: DIL KUĆIŠTE, SIMBOLI

LM248

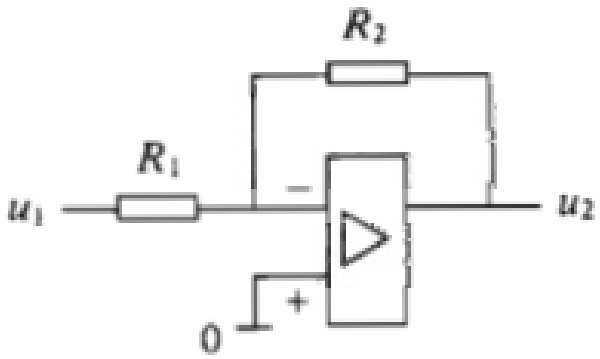




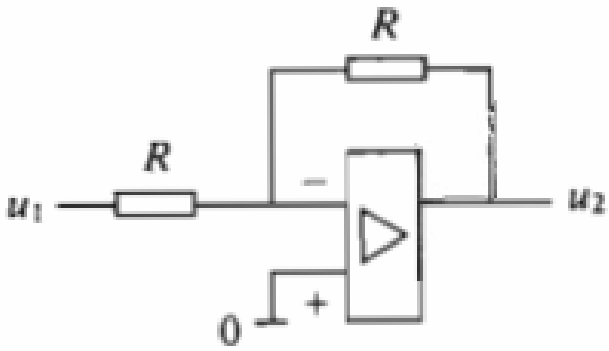
OSNOVNA POJAČAVAČKA KOLA



$$u_2 = -\frac{R_2}{R_1}u_1 + \frac{R_1 + R_2}{R_2}\cdot u_0$$



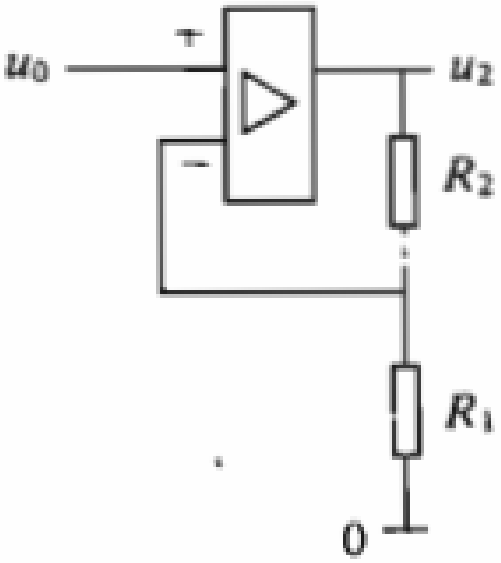
$$u_2 = -\frac{R_2}{R_1}\cdot u_1$$



$$u_2 = -u_1$$

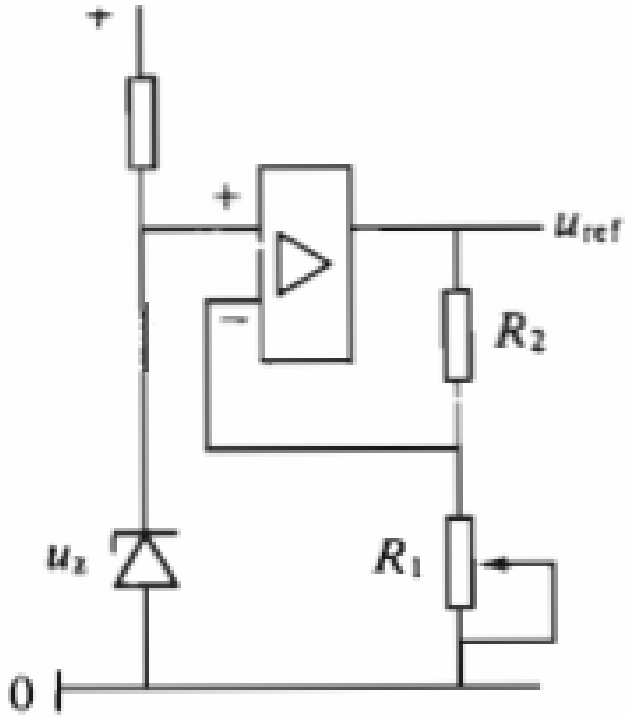
INVERTUJUĆA POJAČAVAČKA KOLA

POJAČAVAČKA KOLA



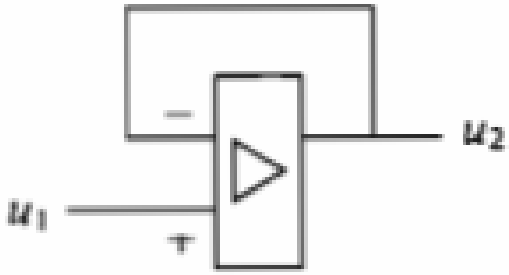
$$U_2 = \frac{R_1 + R_2}{R_1} \cdot u_0$$

NEINVERTUJUĆI POJAČAVAČ



$$u_{ref} = \frac{R_1 + R_2}{R_1} \cdot u_z$$

PRECIZNA REFERENCA



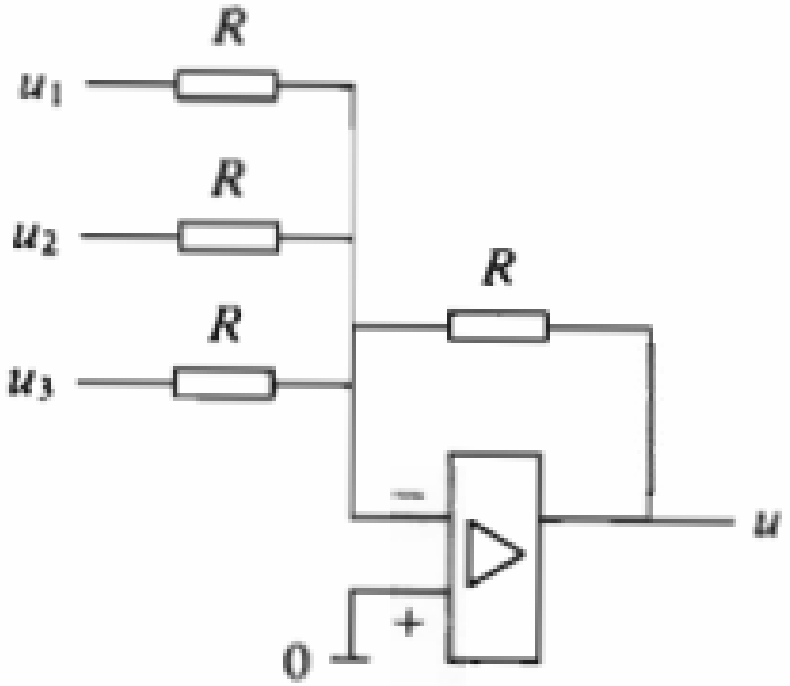
BAFERSKO KOLO

$$R_{in} = \infty$$

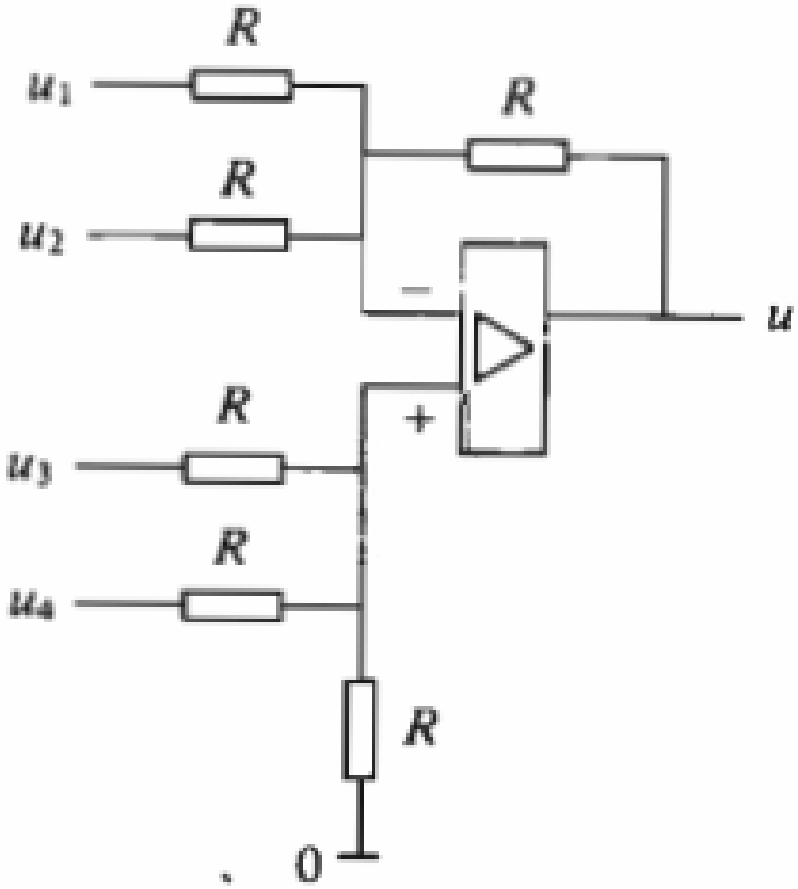
$$R_{out} = 0$$

$$u_1 = u_2$$

SABIRAČI I ODUZIMAČI (kola za sabiranje i oduzimanje)

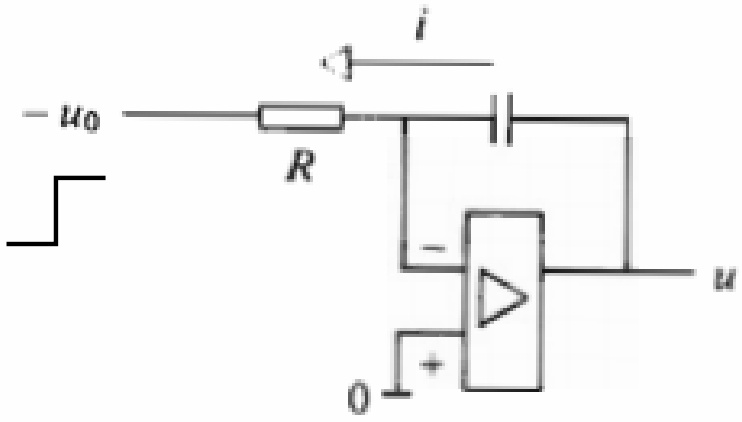


$$u = -(u_1 + u_2 + u_3)$$



$$u = -(u_1 + u_2) + (u_3 + u_4)$$

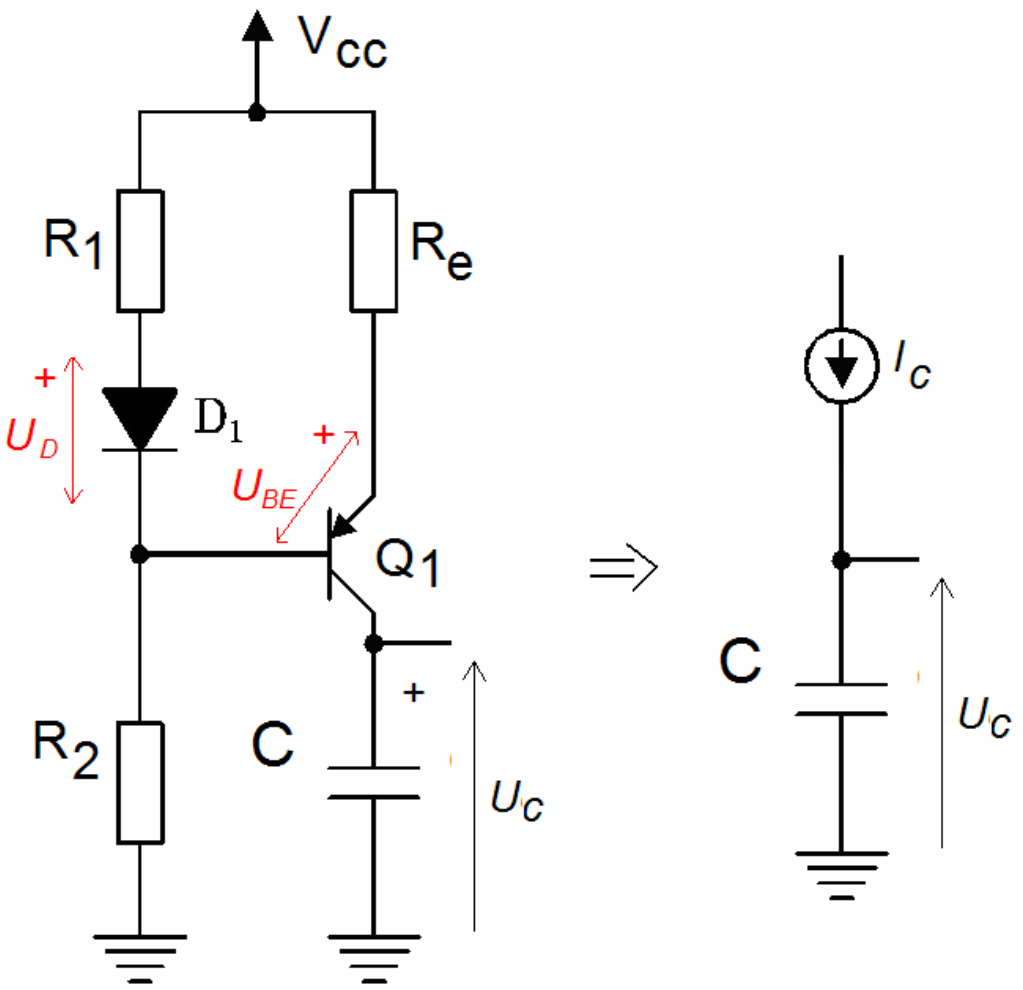
JEDNOSTAVA INTEGRATOR SA OPERACIONIM POJAČAVAČEM



ODZIV NA STEP POBUDU

$$u = \frac{1}{C}\int_0^t i\,\mathrm{d}\tau = \frac{1}{C}\,it = \frac{u_0}{RC}\cdot t$$

DOBIJANJE LINEARNE RAMPE KORIŠĆENJEM STRUJNOG IZVORA



Ako je kolektorska struja tranzistora Q1 relativno mala (<1mA) i ako je njegovo pojačanje relativno veliko ($\beta>200$) njegova bazna struja se može zanemariti u odnosu ostatak kola. Takođe ako je $U_D=U_{BE}$=0.6-0.7V)(realan slučaj) možemo na osnovu prethodno rečenog napisati da je napon na otporniku Re jednak:

$$U_{Re} = \frac{V_{cc} - U_D}{R_1 + R_2} R_1$$

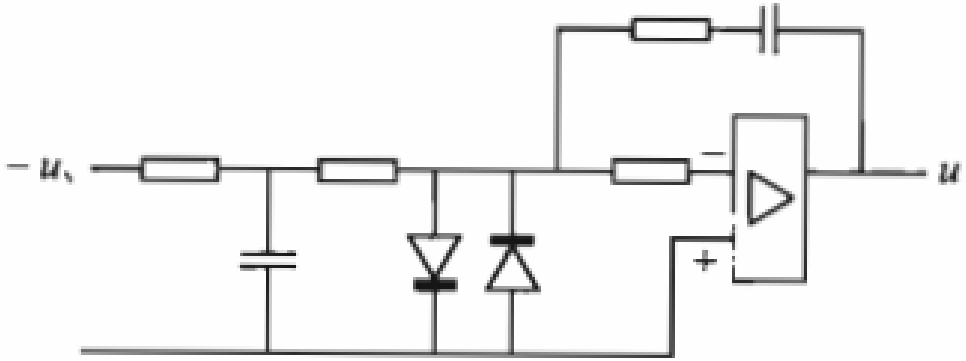
Jednosmerna (konstantna) struja strujnog generatora (kolektorska struja tranzistora Q_1) je jednaka:

$$I_C = \frac{U_{Re}}{R_e}$$

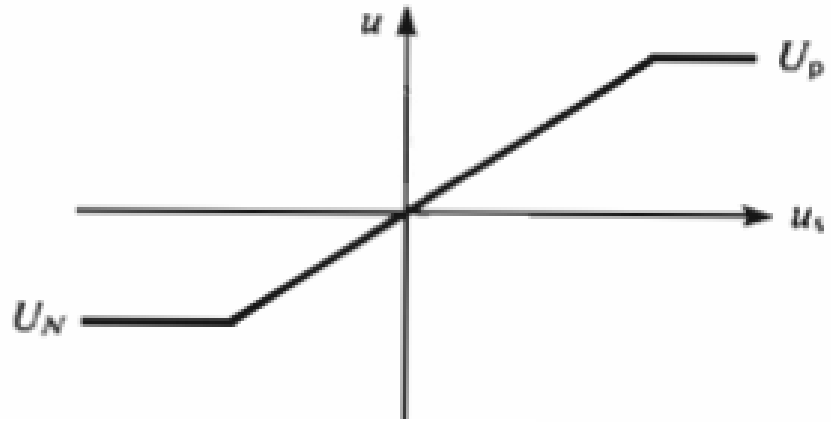
LINEARNA RAMPA

$$u_c(t) = \frac{I_C}{C} \cdot t$$

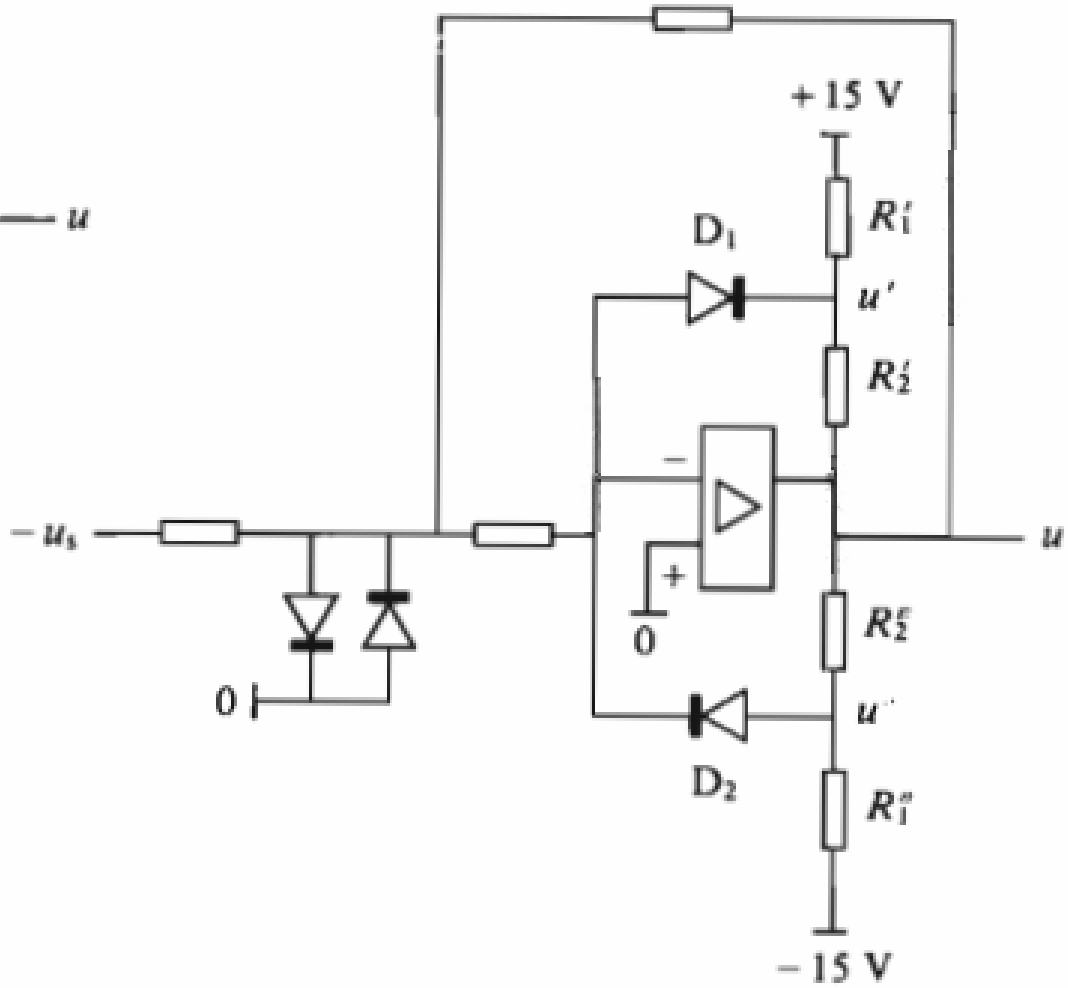
PI regulator



El. Šema bez ograničenja izlaza

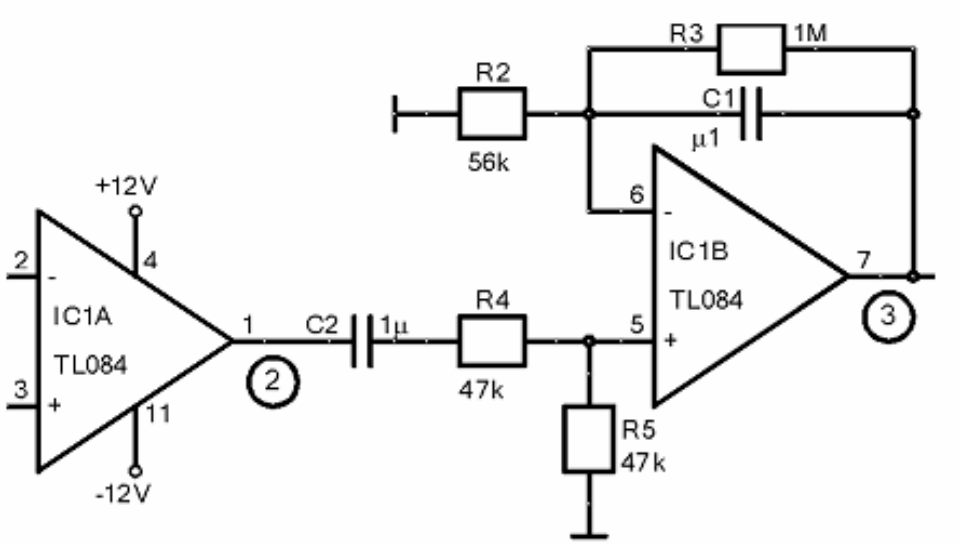


Prenosna funkcija
(uočiti ograničenje nivoa)

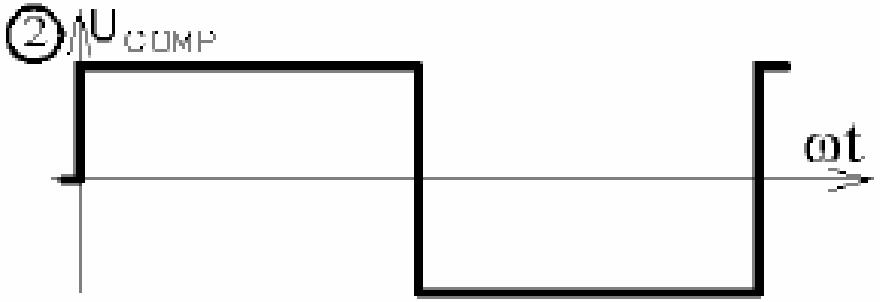


PI regulator sa implementiranim ograničenjem

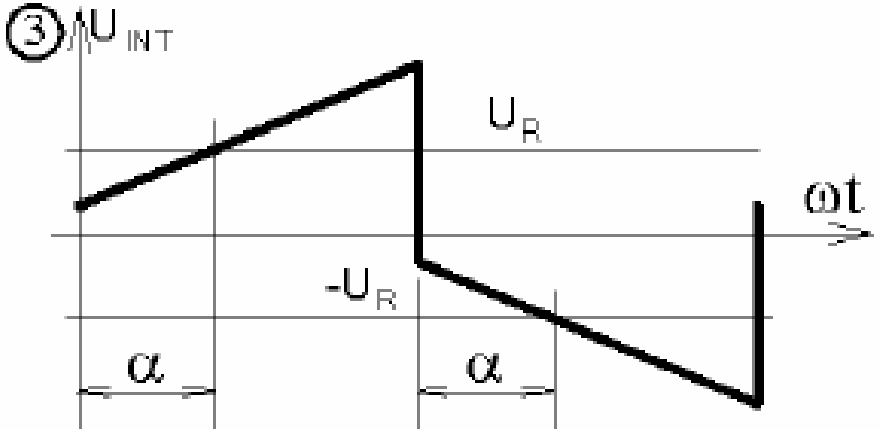
TIPIČNA PRIMEA INTERGRATORA U UPRAVLJAČKIM KOLIMA ENERGETSKIH PRETVARAČA: INTEGRACIJA SINHRONIZACIONOG NAPONA



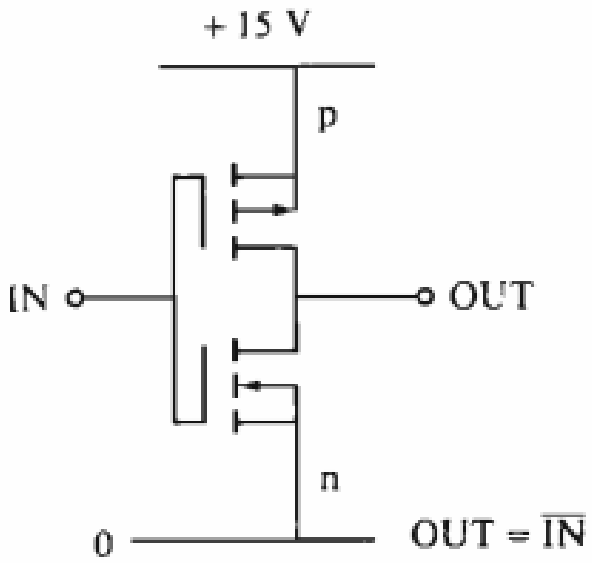
NAPON SINHRONIZOVAN SA MREŽOM



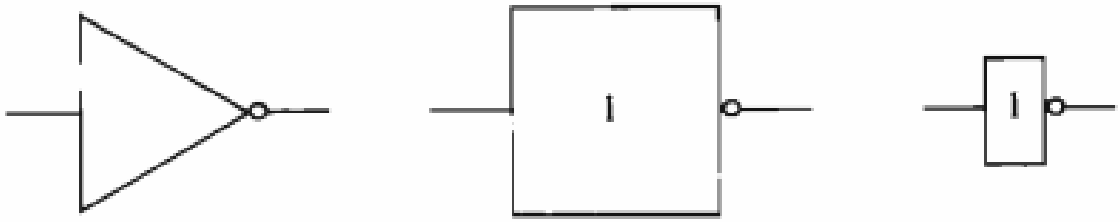
IZLAZ INTEGRATORA



CMOS invertor



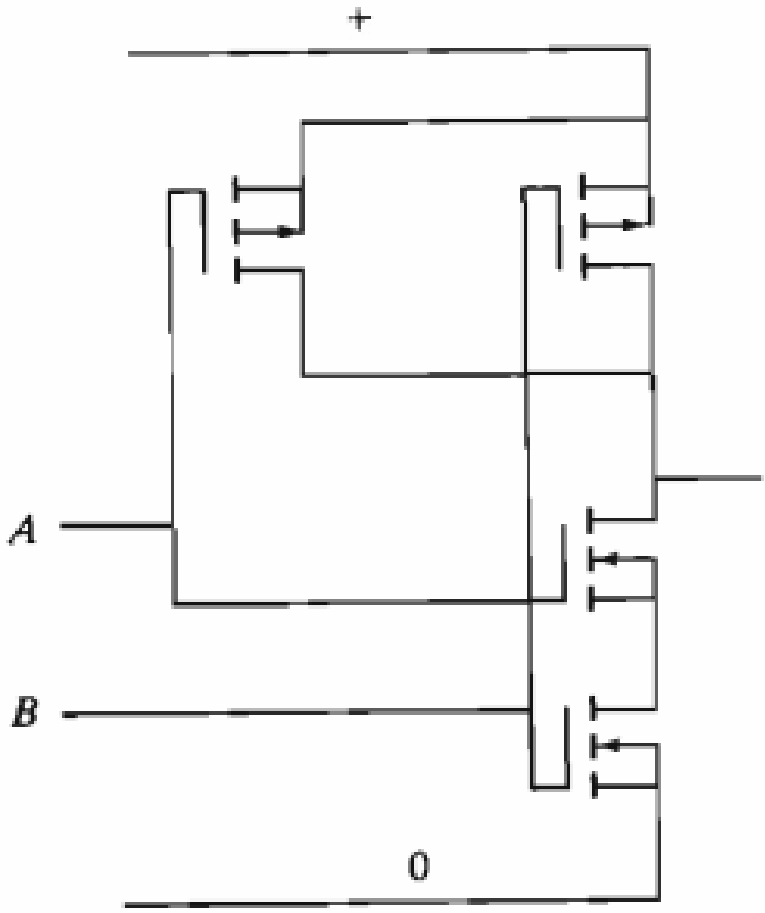
el.kolo



simboli

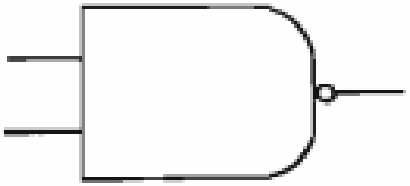
CMOS logičko NI kolo

TABLICA ISTINITOSTI

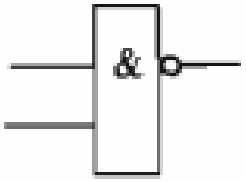


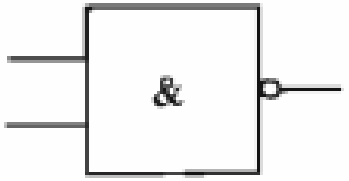
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

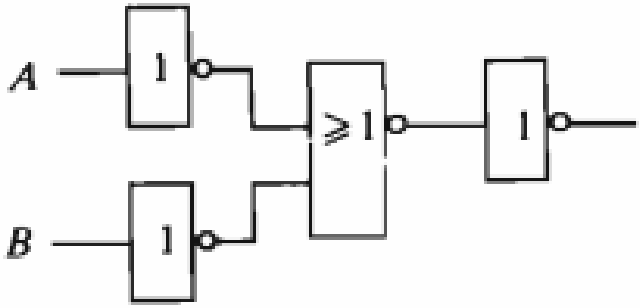
$C = \overline{A \times B}$



NAND

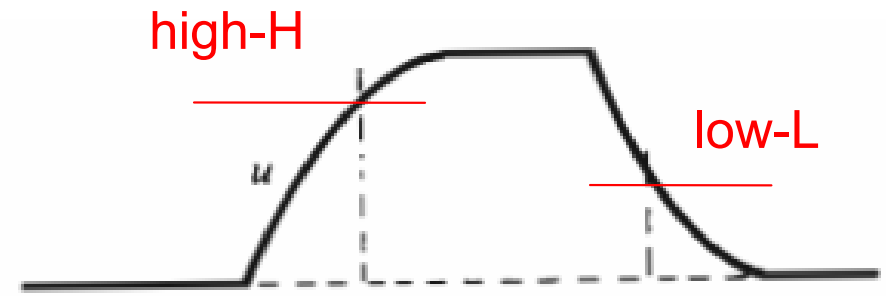


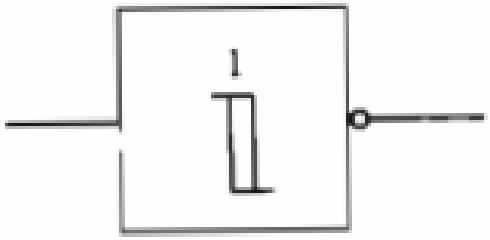


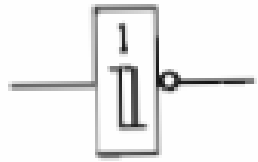


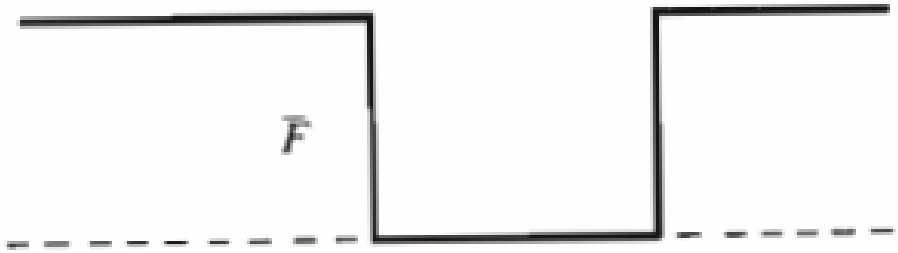
$C = \overline{\overline{A} + \overline{B}} = \overline{A \times B}$

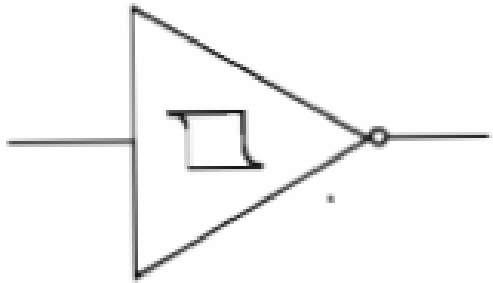
ŠMIT TRIGER (INVERTOR)



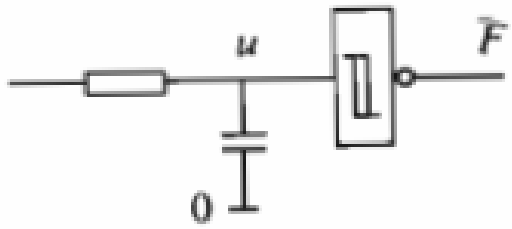






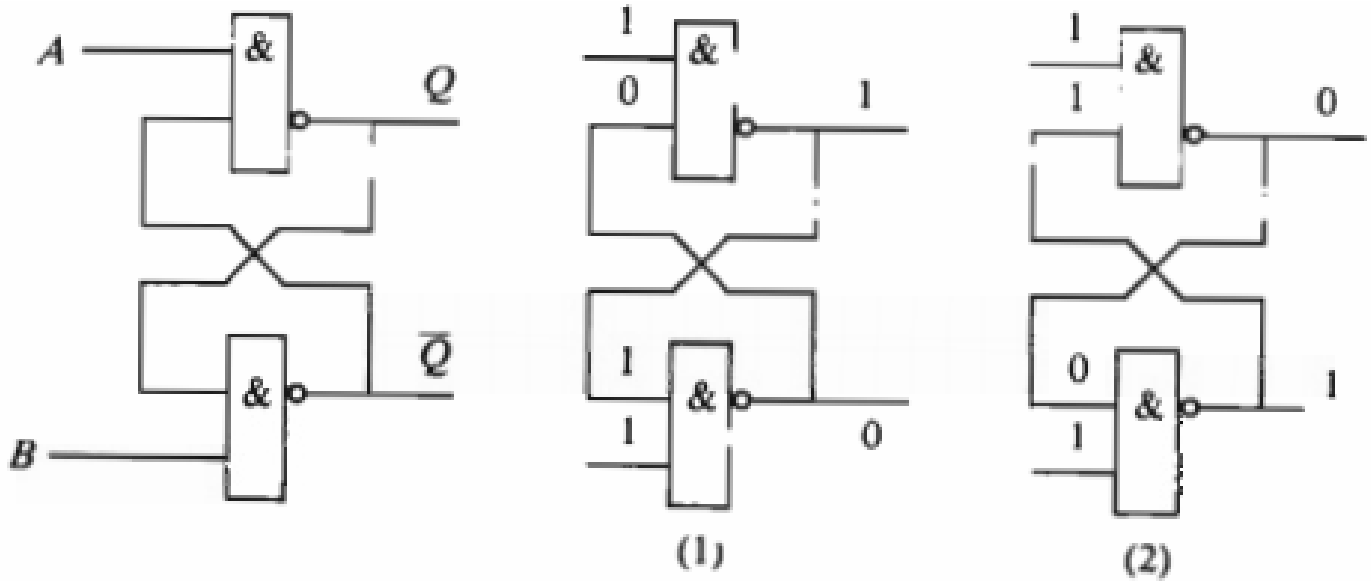


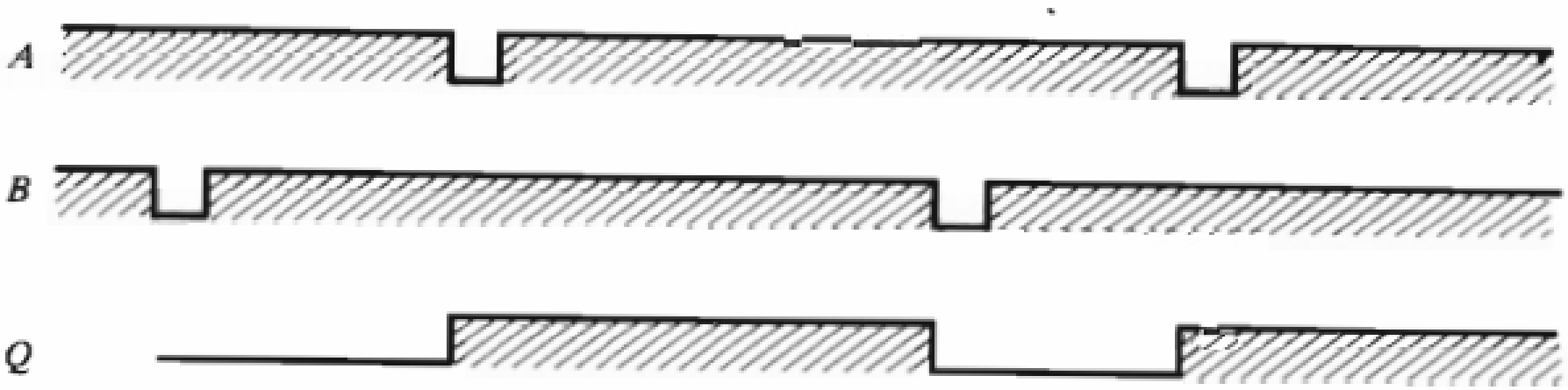
SIMBOLI



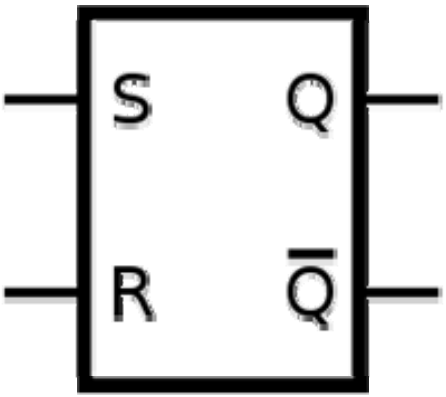
RC kolom se ostvaruje kašnjenje

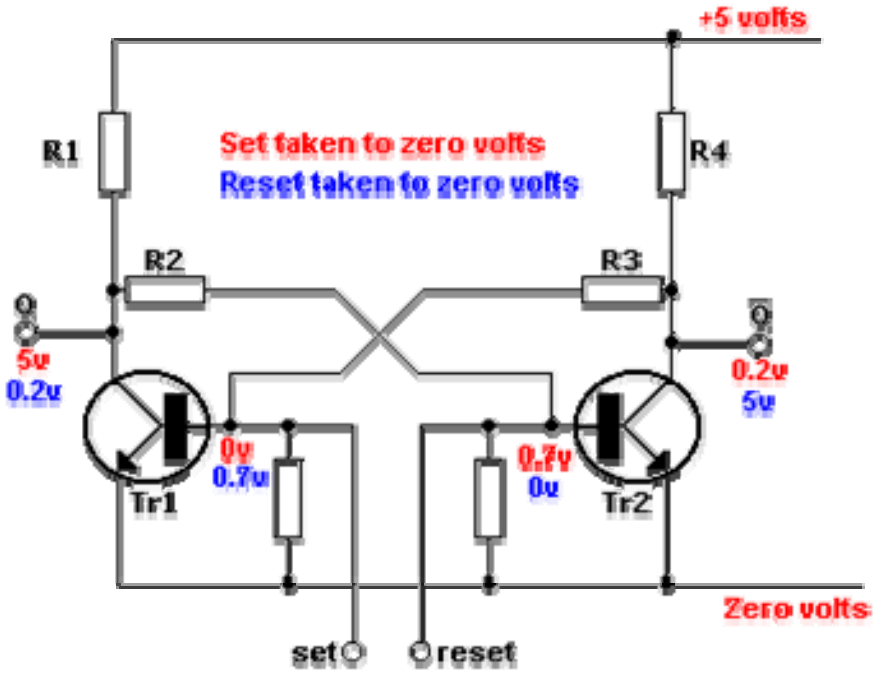
FLIP-FLOP

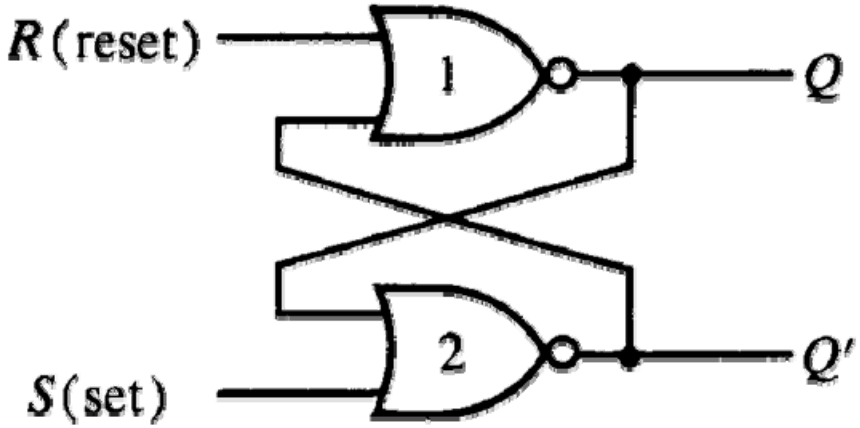




RS flip-flop







S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

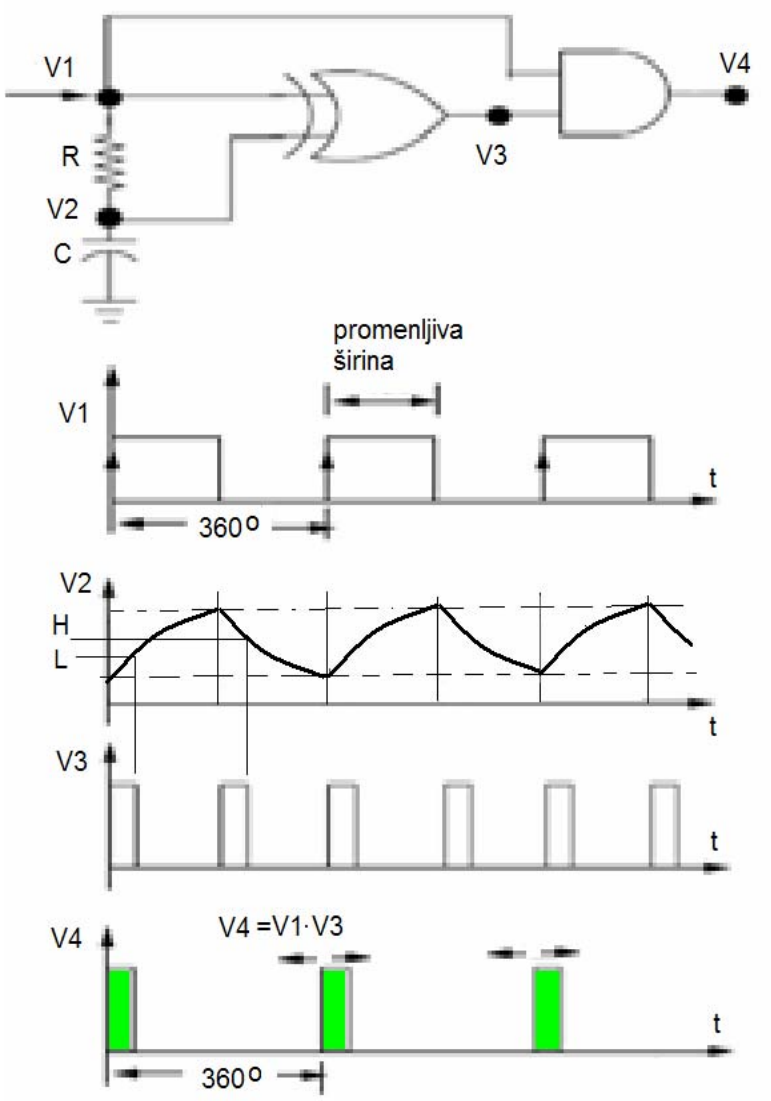
LOGIČKO KOLO

TABLICA ISTINITOSTI

Princip rada CMOS MONOSTABILNOG KOLA

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Ekskluzivno ILI kolo i njegova tablica istinitosti

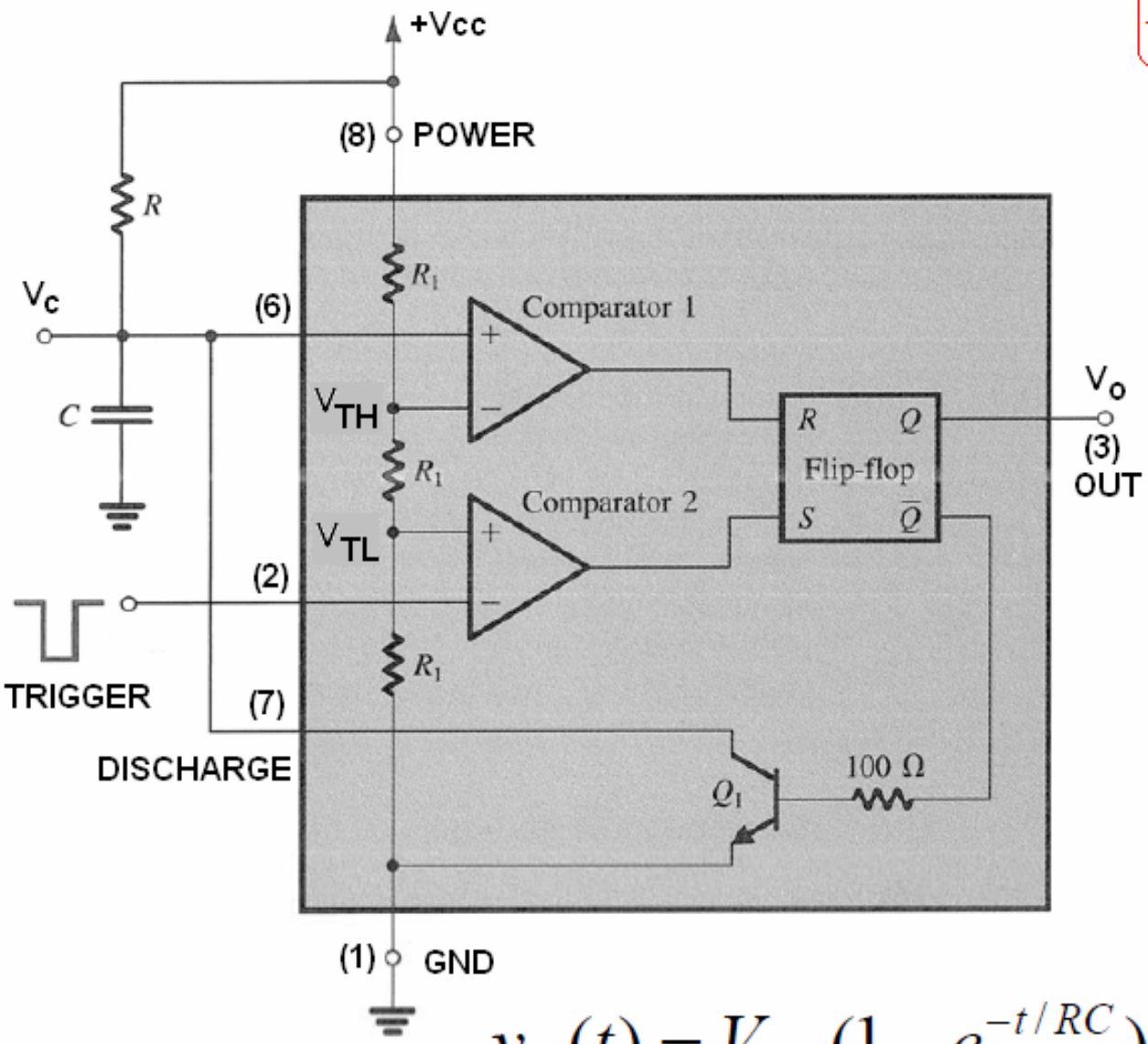


Predstavljeno monostabilno kolo uobličava impulse V1. Ovi impulsi su promenljive širine i recimo da su posledica poređenja referentnog signala i signala rampe (slajd 4)

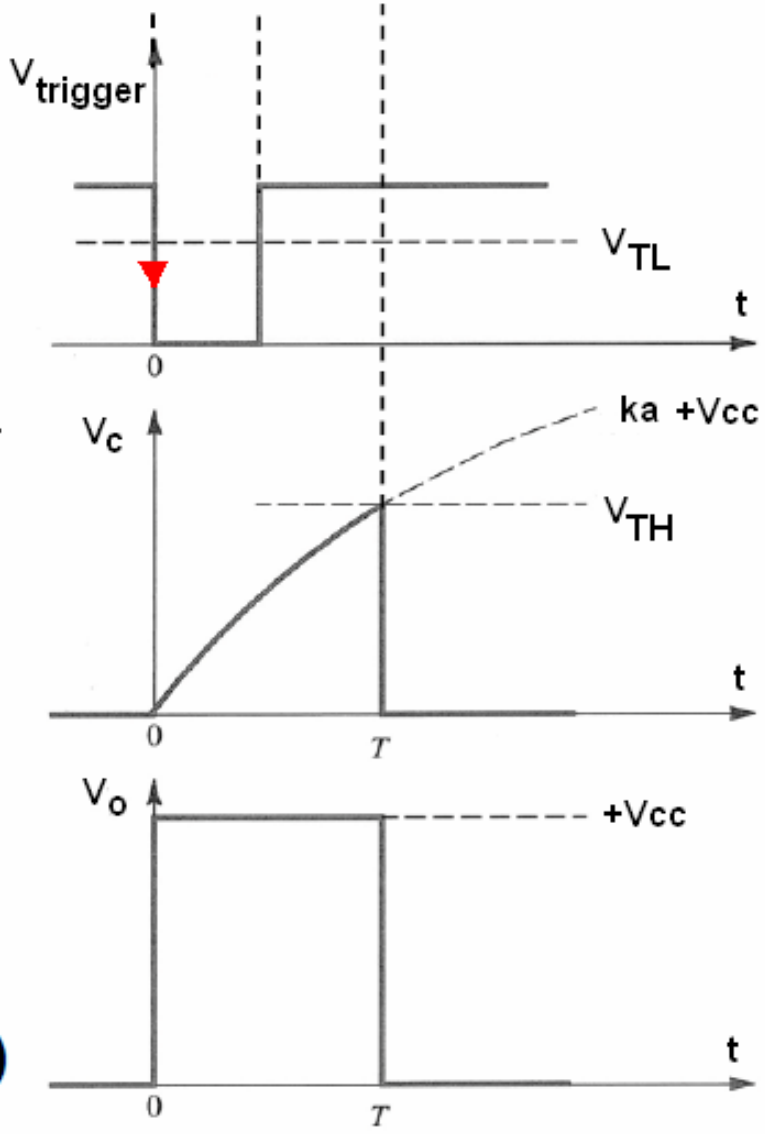
Ulazno EX ILI kolo detektuje uzlaznu i silaznu ivicu signala V1 i na izlazu daje signal V3 čije je trajanje značajno kraće od širine Impulsa V1. Ovo trajanje je određeno vremenskom konstantom RC kola.

Korišćenjem “I” kola, odnosno formiranjem logičke funkcije V1·V3, dobija se signal V4 koji ustvari predstavlja signal detekcije uzlazne ivice signala V1.

TAJMER NE555 (kao monostabilni multivibrator)



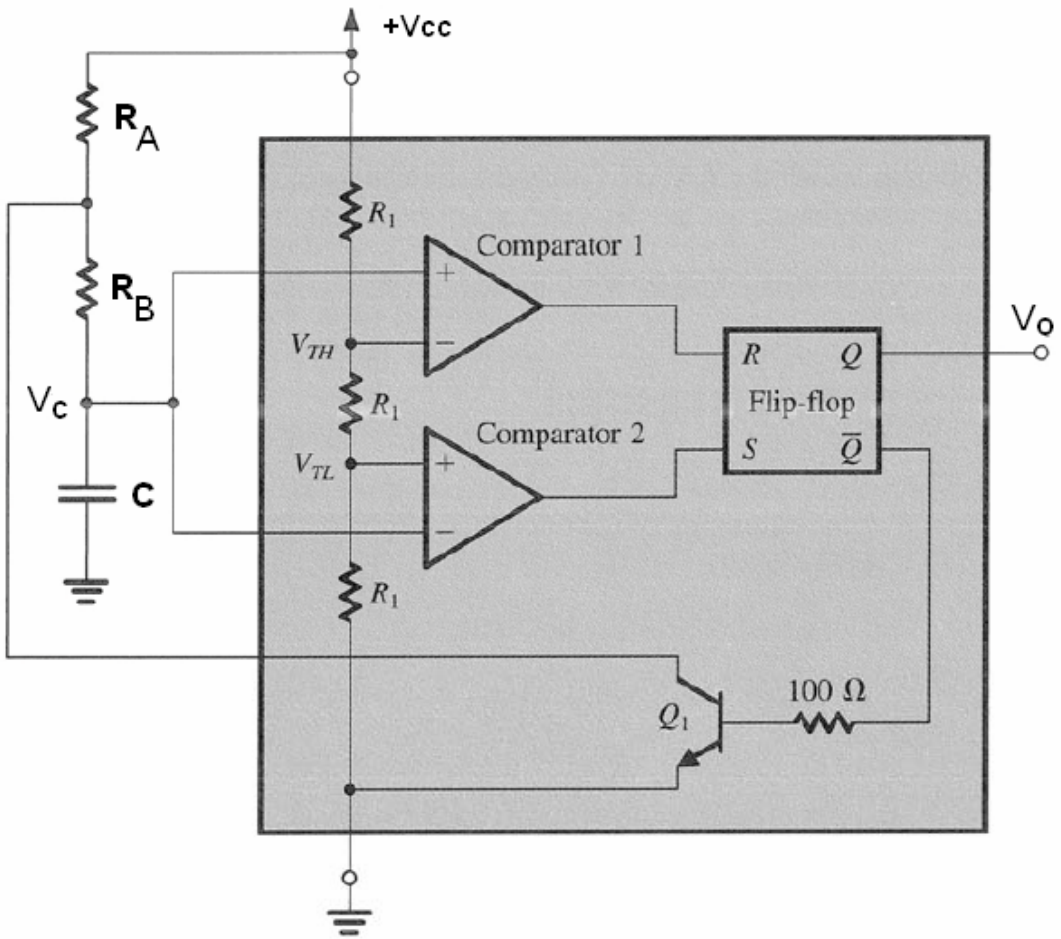
S	0	1	0	0 → 0
R	0	0	0	1 → 0

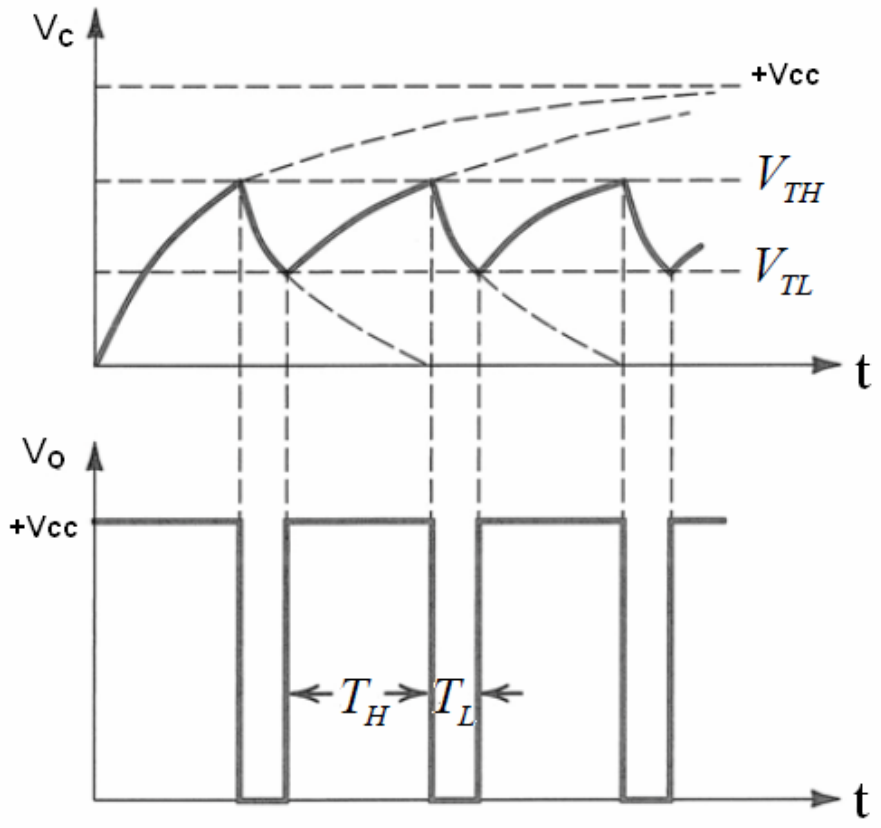


$$v_C(t) = V_{CC}(1 - e^{-t/RC})$$

$$T = RC\ln 3 \approx 1.1RC$$

TAJMER NE555 (kao astabilni multivibrator)





$$v_C(t) = V_{CC} - (V_{CC} - V_{TL})e^{-t/C(R_A+R_B)}$$

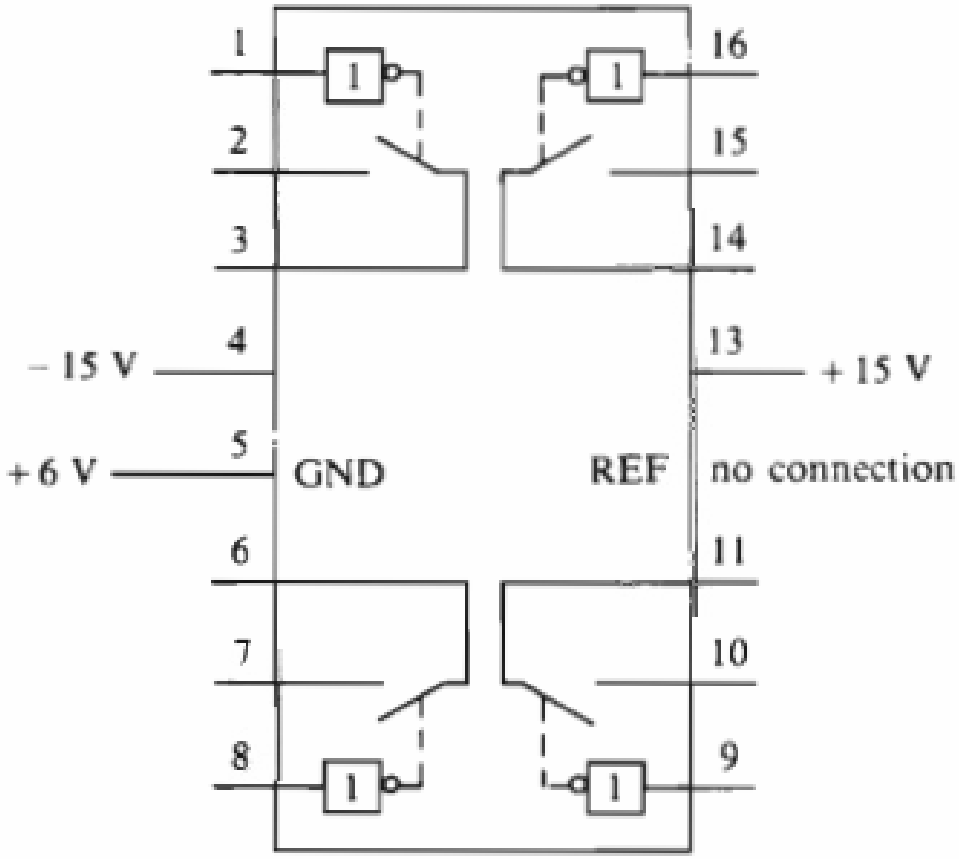
$$T_H = C(R_A + R_B)\ln 2 \approx 0.69C(R_A + R_B)$$

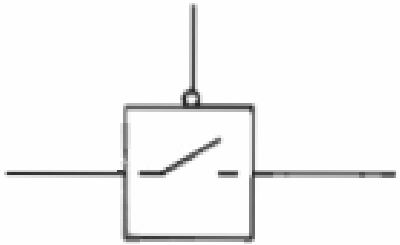
$$v_C = V_{TH}e^{-t/CR_B}$$

$$T_L = CR_B \ln 3 \approx 0.69CR_B$$

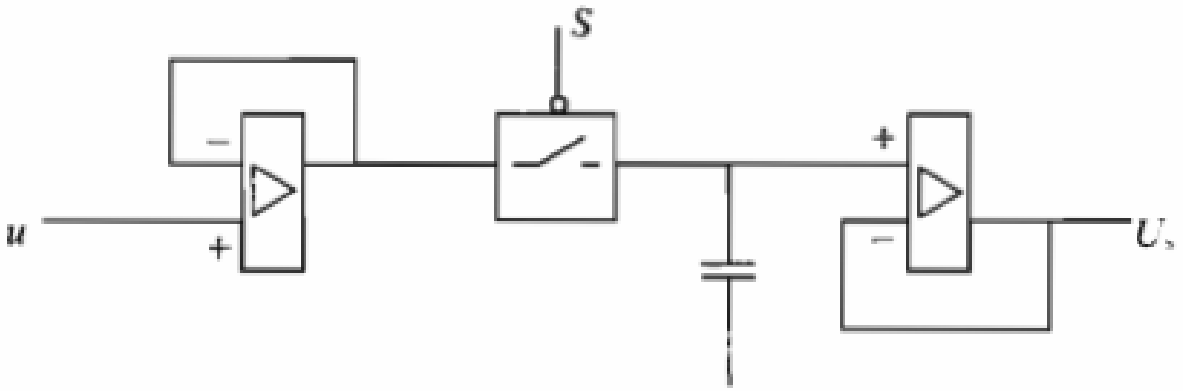
$$T = T_H + T_L = 0.69C(R_A + 2R_B)$$

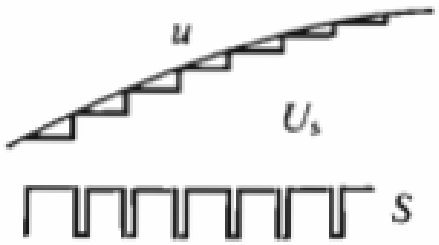
$$\mathrm{D} \equiv \frac{T_H}{T_H + T_L} = \frac{R_A + R_B}{R_A + 2R_B}$$



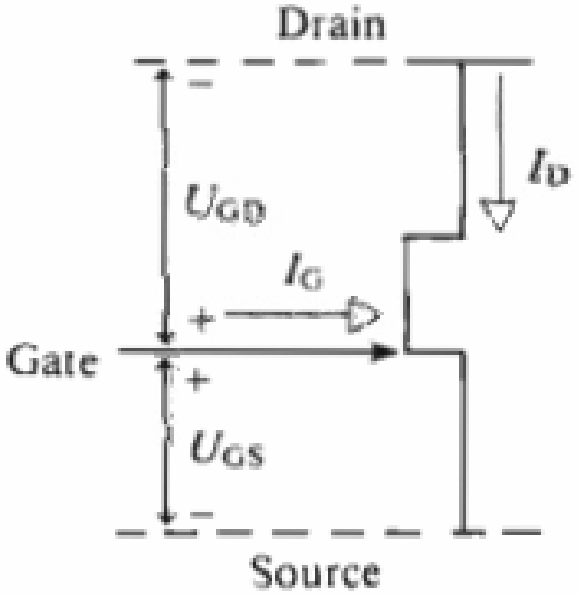


ANALOGNI PREKIDAČ



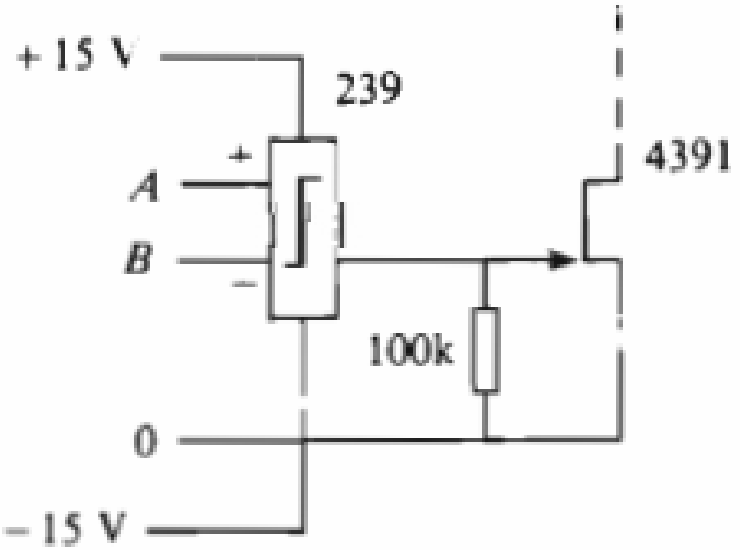


FET KAO ANALOGNI PREKIDAČ



Maximum voltage $-U_{GS}$	$= -U_{GD} = 40$ V
Maximum gate current I_G	$= 50$ mA
Maximum pinch-off voltage $-U_p$	$= 10$ V
$R_{DS} \leqslant 30\ \Omega$ for $U_{GS} = 0$ and I_D	$= 1$ mA
$I_D = 50 - 150$ mA for $U_{DS} = 20$ V and $U_{GS} = 0$	

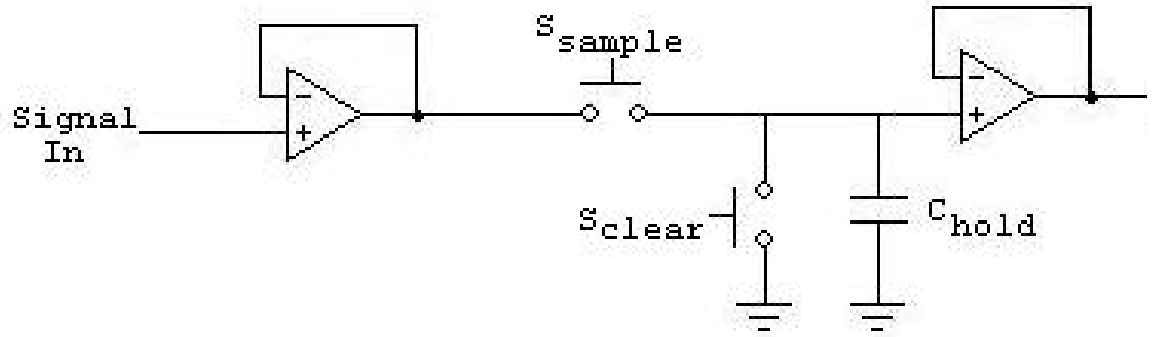
Tipični parametri FET-a



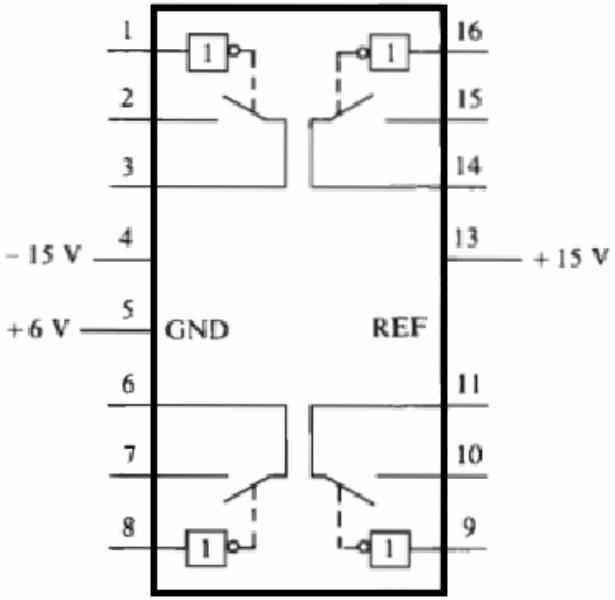
za A > B: ON

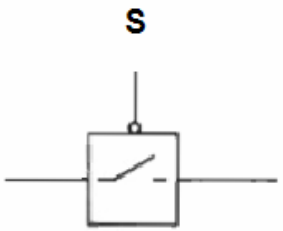
za A < B : OFF

TIPIČNA PRIMENA ANALOGNOG PREKIDAČA: SAMPLE & HOLD kolo



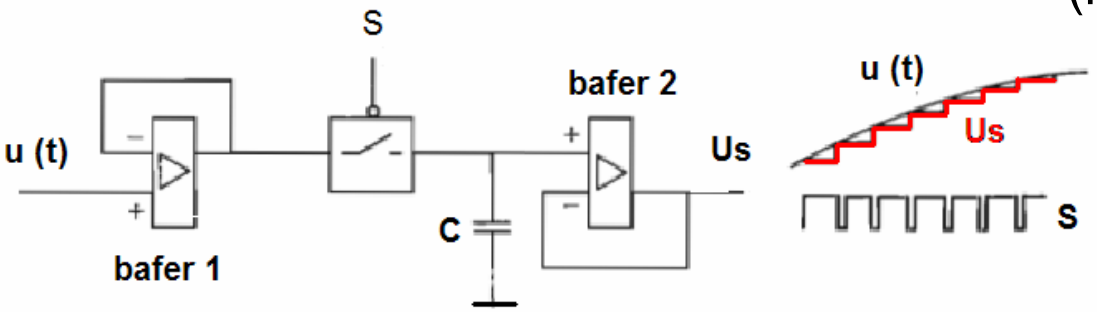
-Hold kondenzator drži napon čak i kada
-Ssample deluje kratkotrajno!!!
-Pražnjenje hold kondenzatora se ostvaruje sa Sclear





analogni prekidač

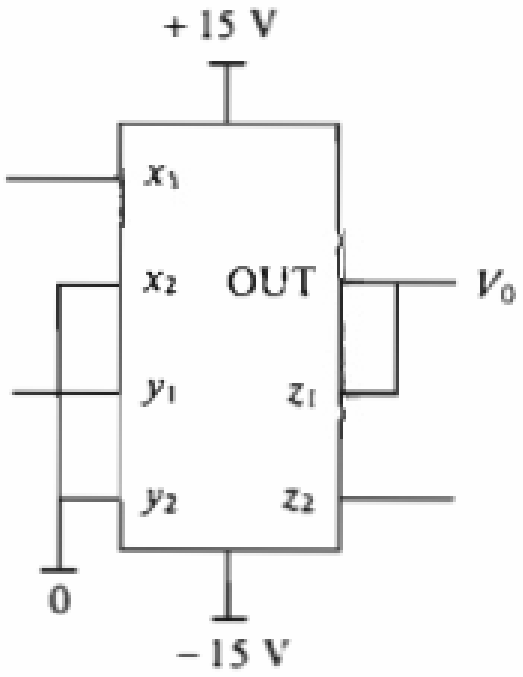
-Korišćenje analognog prekidača umesto mehaničkih.
-ANALOG SWITCH (kontrolisan je naponom)



ANALOGNI MNOŽAČ

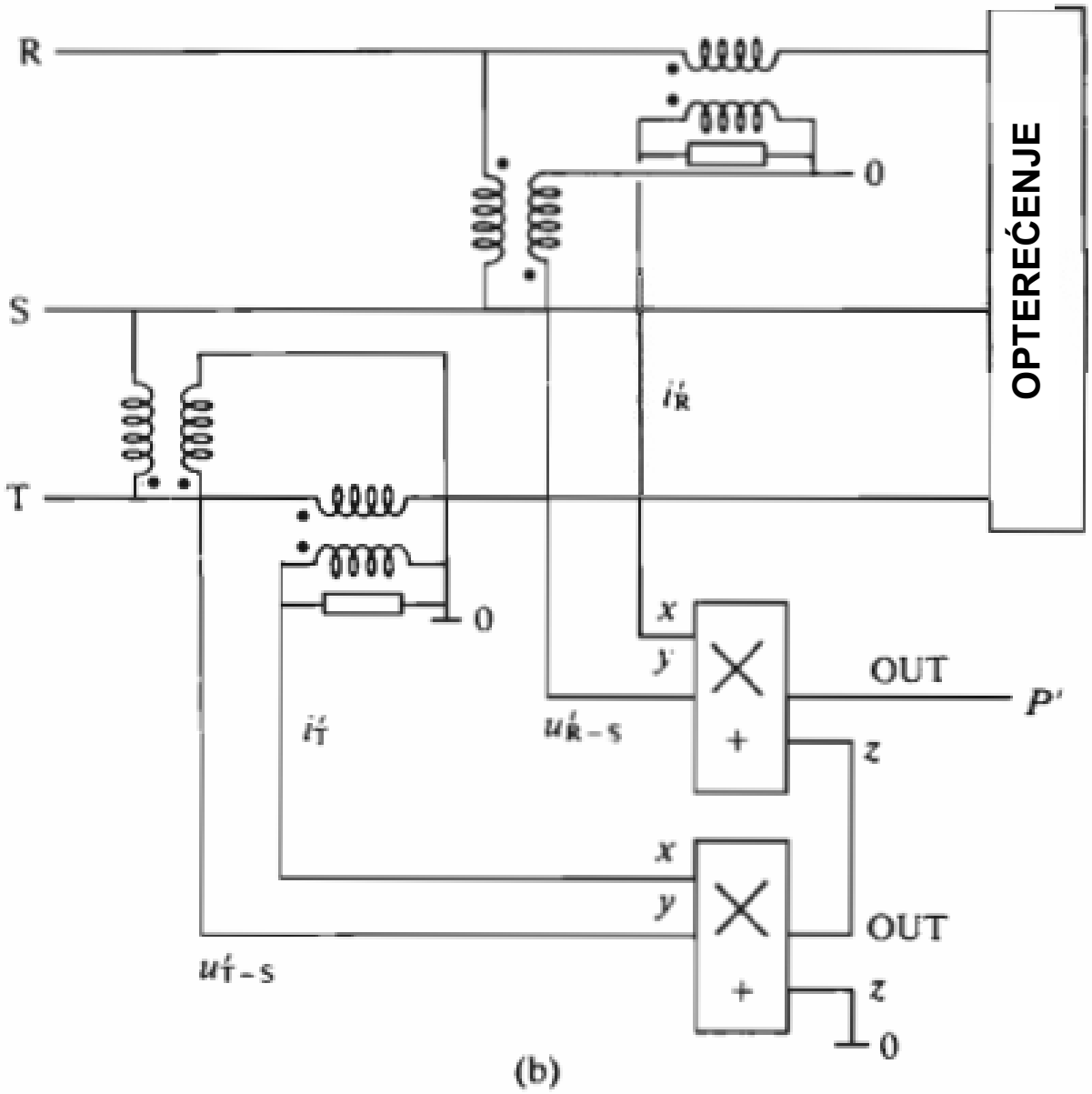
$$V_0 = \frac{1}{T}\int^{T} u'_{R-S}\, i'_R \, dt + \frac{1}{T}\int^{T} u'_{T-S}\, i'_T \, dt$$

$$V_0 = \frac{x_1 y_1}{10} + z_2$$



(a)

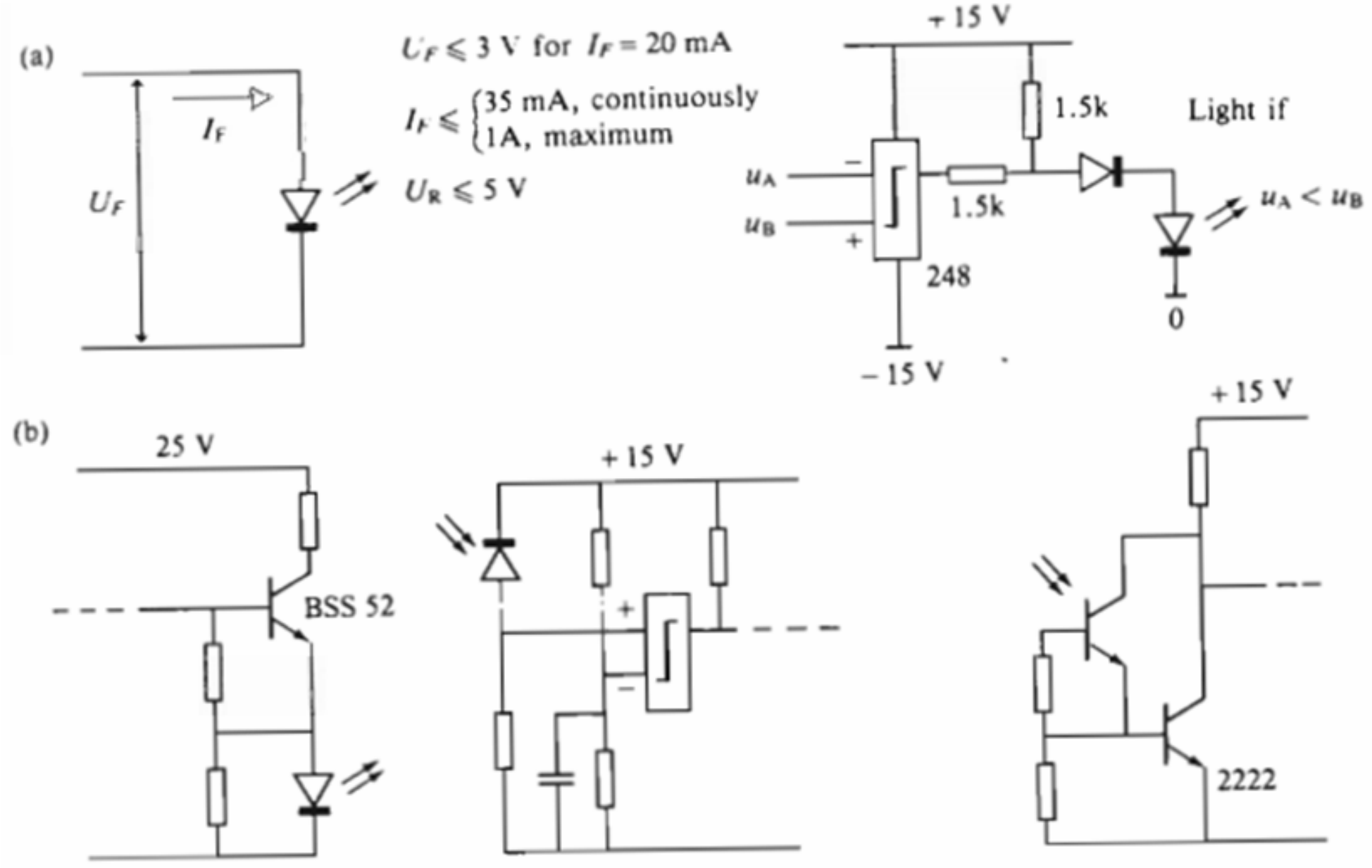
SIMBOL



(b)

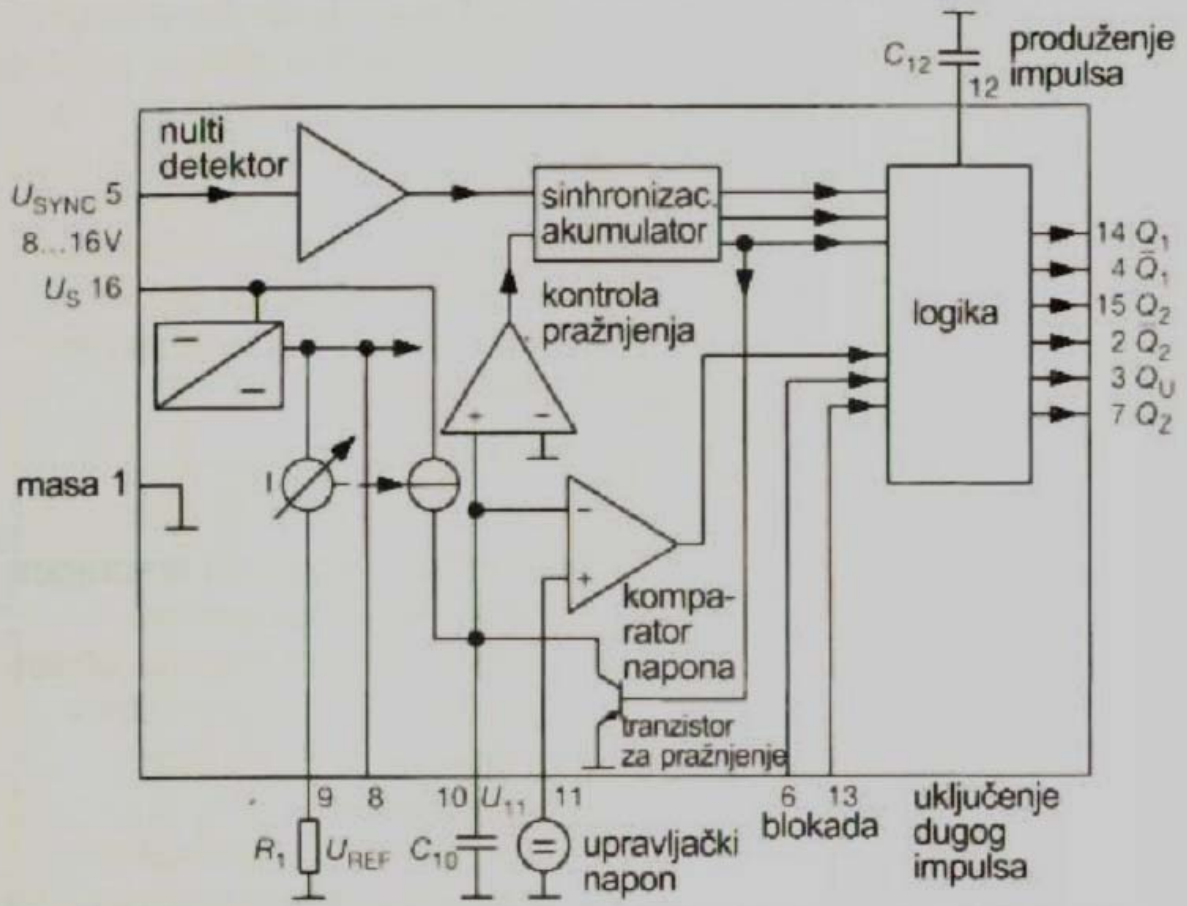
ANALOGNI MNOŽAČ: TROFAZNO MERENJE SNAGE

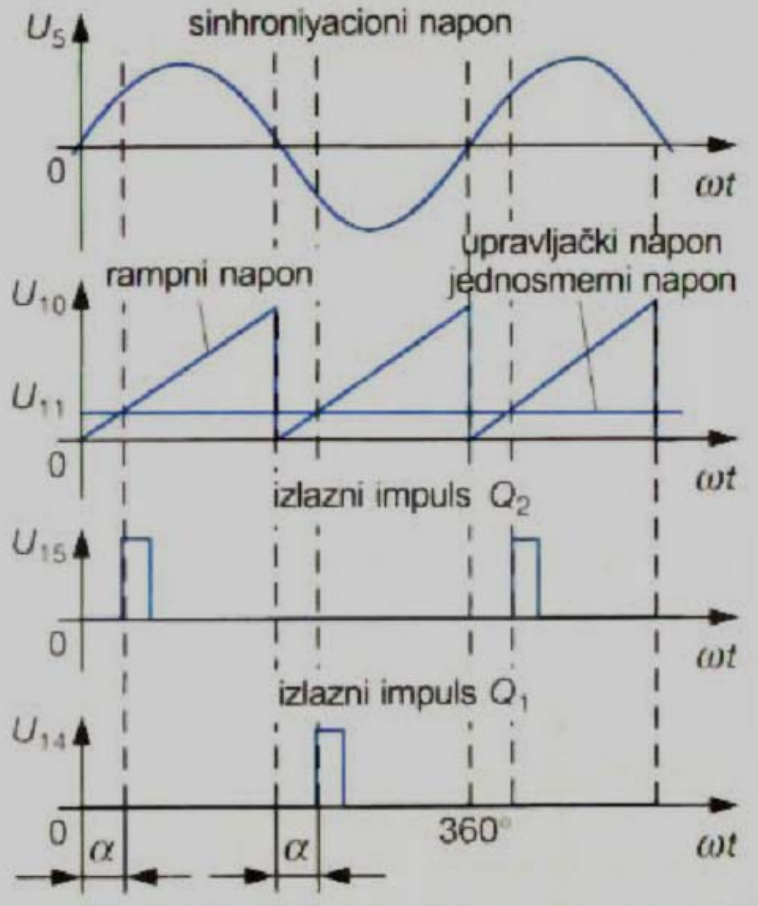
OSNOVNA OPTIČKA KOLA ZA PRENOS SIGNALA



Transmiter (predajnik) sa LED i prijemnik sa foto diodom ili foto tranzistorom

Integrisana kola (sklop) za fazno upravljanje (upravljanje otsecanjem faze) npr. TCA 785

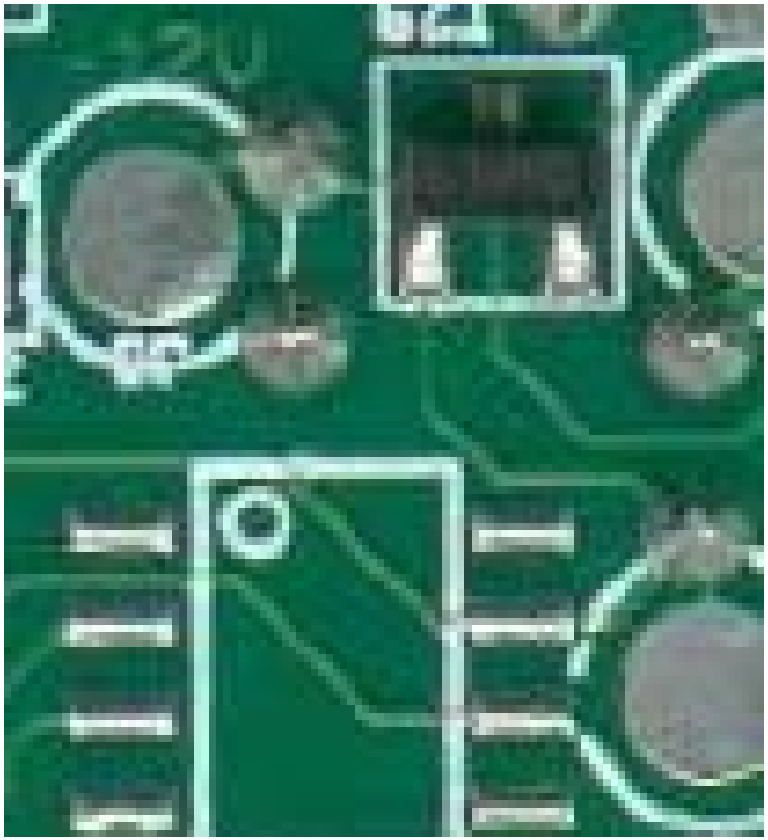


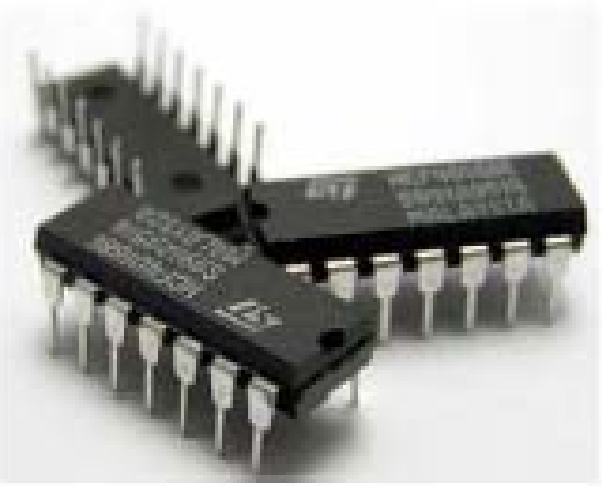


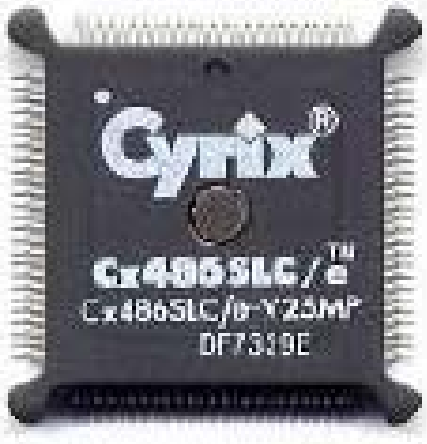
Primena	Opis
• Fazno upravljanje ventilima u ispravljačkim sklopovima i pozicionerima. • Moguć je trofazni pogon sa 3 integrisana kola. • Može se koristiti kao nulta sklopka kod upravljanja paketom titraja.	• Dobijanje sinhronizacionog napona iz mrežnog napona. • Izvor konstantne struje I puni C_{10} vremenski linearno • Kada je $U_{10} > U_{11}$, onda se deblokiraju izlazni impulsi Q_1 i Q_2. • Produženje trajanja impulsa preko C_{12}.

HVALA NA PAŽNJI!!

PITANJA?







JANUAR 2014